INSTRUCTION
MANUAL

Programmable
Digital Delay Generator
Model 7040

BNC BERKELEY NUCLEONICS CORP.

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Programmable
Digital Delay Generator
Model 7040

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Warranty

Berkeley Nucleonics Corporation warrants all instruments, including component parts, to be free from defects in material and workmanship, under normal use and service for a period of one year. If repairs are required during the warranty period, contact the factory for component replacement or shipping instructions. Include serial number of the instrument. This warranty is void if the unit is repaired or altered by others than those authorized by the Berkeley Nucleonics Corporation.

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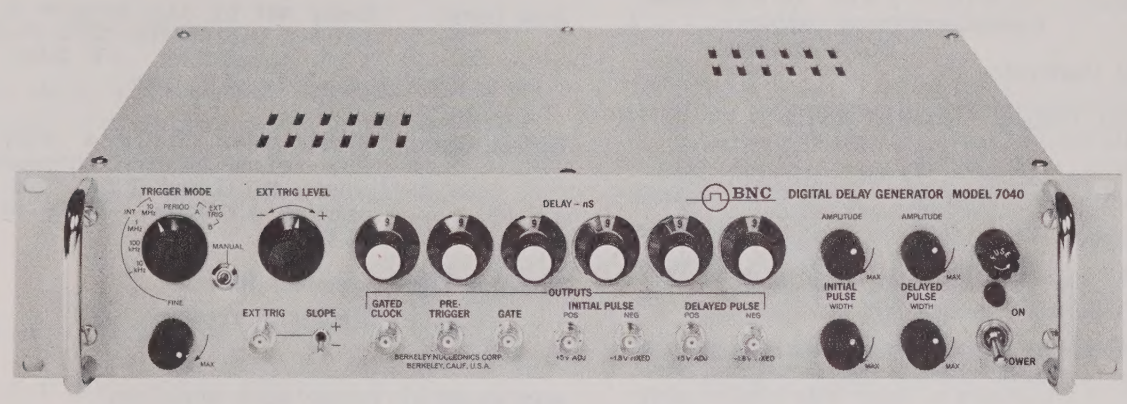
SECTION 1

SPECIFICATIONS



DIGITAL DELAY

(Between Initial and Delayed Pulse)

Range: 0 to 999.999 μs in 1 ns increments. Six decade front panel switches or external programming.

Accuracy: 1 - 9 ns, ± 0.1 ns;

10 - 99 ns, ± 0.2 ns;

100 ns - 999.999 μs, ± 0.5 ns or ± (2 x 10^{-7} / °C) x delay, whichever is greater.

Stability: 1 x 10^{-7} x delay / week or ± 10 ps / week, whichever is greater.

Jitter: 0 - 99 ns, ± 50 ps
100 ns - 999.999 μs, ± 100 ps.

INITIAL OUTPUT PULSES

(Beginning of adjustable delay period)

Positive: Amplitude, 0.5 V to 5 V into 50 Ω, continuously adjustable;

Width, 15 ns to 1 μs, continuously adjustable;

Rise time, 3 ns.

Negative: Amplitude, -1.8 V fixed amplitude from 50 Ω; or -0.9 V into 50 Ω;

Width, 15 ns to 1 μs, continuously adjustable;

Rise time, 2 ns.

DELAYED OUTPUT PULSE

Positive: Same as Positive Initial Pulse

Negative: Same as Negative Initial Pulse

GATE OUTPUT

Width: Same as spacing between Initial and Delayed Pulses ± 2 ns.

Amplitude: +2.5 V into 50 Ω

Rise Time: 3 ns

GATED CLOCK OUTPUT

Signal: 100 MHz Pulse Train

Amplitude: +2 V into 50 Ω

Number of Gated Cycles: Equal to setting of the five most significant digits of delay switches or external programming. For Example: A delay setting of 3458 ns, the number of clock pulses is 345.

PRE-TRIGGER OUTPUT

Time of Occurrence: 45 ns before Initial Pulse

Amplitude: +1.5 V into 50 Ω

Width: 10 ns

Rise Time: 4 ns

TRIGGER MODES

Internal

Rate: 0.5 kHz - 5 MHz, in 4 decades, continuously adjustable

Manual Pushbutton

External Trigger - Mode A* and B**

Rate: 0 - 5 MHz

Minimum Amplitude: 200 mV DC coupled

Trigger Level Control: ± 1 V variable

Slope: Selectable, positive or negative

Input Impedance: 50 Ω

* Mode A: Delay between external trigger and initial pulse is approximately 75ns. Updating of delay data occurs after the leading edge of the delayed pulse.

**Mode B: Delay between external trigger and initial pulse is approximately 250 ns. Updating of delay data occurs before the pre-trigger out.

Jitter: Between external trigger and initial output pulse, ± 5 ns. Non-synchronous gating of 100 MHz clock.

Period: Provides mode of operation with a period equal to the five most significant digits of delay setting + 200 ns. Same accuracy as Digital Delay.

REMOTE PROGRAMMING

(Amphenol 57-40360 connector on rear of chassis.)

Data Input: Delay set by six decades of 1-2-4-8 BCD levels. DTL and TTL compatible; 0 V false, +2.5 V to +5 V true.

Update Input: Update pulse changes delay data before external trigger pulse. DTL and TTL compatible; 0 V false, +2.5 V to +5 V true.

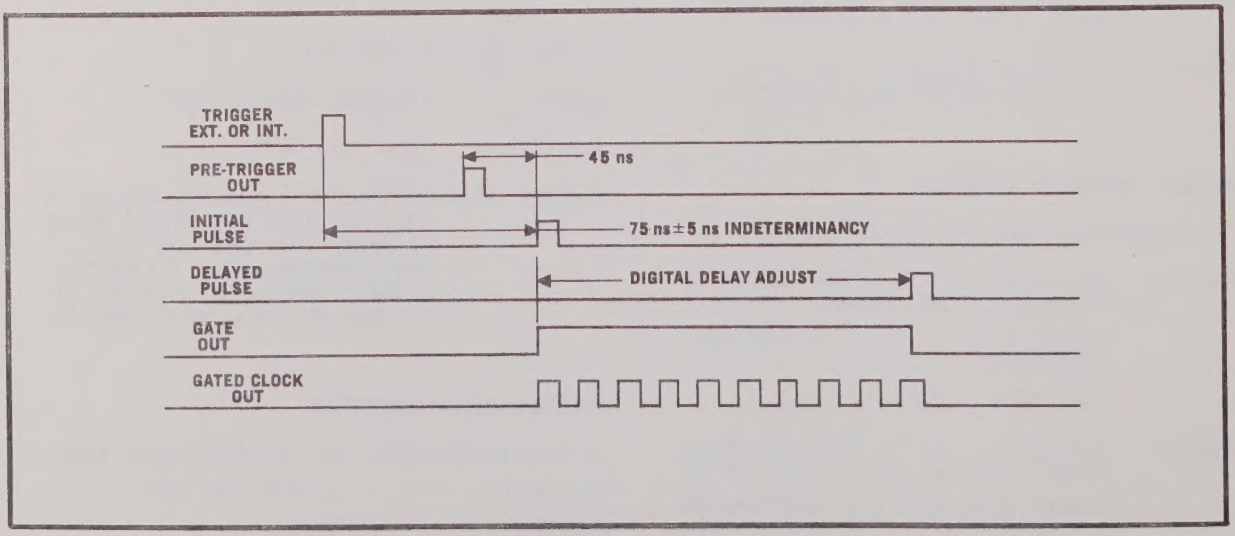
Updating (Programming) Rate:
1 MHz or greater.

MECHANICAL (Relay Rack Mounting)
19" wide x 3-1/2" high x 12-1/8" deep.

AMBIENT: 0^{o}C to 55^{o}C

POWER: 115 or 230 VAC ± 10%, 50 - 60 Hz, 45 W

WEIGHT: 13 lbs, net; 19 lbs, shipping.



Input and Output Waveforms of the Model 7040.

SECTION 2
OPERATING INFORMATION

2.1 GENERAL

To aid in understanding the capabilities of the Model 7040 Programmable Delay Generator, this section describes the operation of front and rear panel connectors and controls.

2.2 GENERAL INFORMATION

2.2.1 OPERATING TEMPERATURE

The Model 7040 is convection cooled by holes in the top, sides, and bottom of the instrument. The sides of the instrument should be allowed at least 2" clearance. The top and bottom holes should not be covered.

Turn on the Model 7040 thirty minutes prior to use to allow temperature sensitive components to reach their quiescent state.

2.2.2 CABLES, ATTENUATORS, AND SCOPES

The various outputs of the Model 7040 Programmable Delay Generator contain frequency components in excess of 250 MHz. All signal handling components such as loads, attenuators, cables, connectors and oscilloscopes should have a flat response exceeding 250 MHz. A load, cable or attenuator mismatch will cause reflections which may result in errors in the measured delays. Some sampling oscilloscopes have maximum input ratings that are exceeded by the outputs on the Model 7040, and the use of attenuators is required to protect the scope.

2.2.3 GENERAL PERFORMANCE INFORMATION

(1) Since there generally is no synchronization between a trigger (external or internal) and the 100 MHz clock in the Model 7040, there is a ± 5 ns indeterminancy between the trigger and the Initial Pulse. By using the PRE-TRIGGER pulse as a trigger for the instruments or circuits to be checked, this indeterminancy is avoided. The PRE-TRIGGER pulse is synchronized to the system clock and delay jitter with respect to the PRE-TRIGGER is then only ± 100 ps. The PRE-TRIGGER pulse occurs 45 ns before the INITIAL PULSE.

(2) The calibration of the Model 7040 is made with delays measured from the 50% point of the leading edge of the INITIAL PULSE to the 50% point of the leading edge of the DELAYED PULSE. These measurements are made at the output connectors. The effect of cables at these connectors on delay calibration should always be considered. For example, one foot of RG/58 has a delay of about 1.5 ns. The selection of pulse polarity or amplitude has no effect on the delay accuracy.

2.3 OPERATING CONTROLS AND CONNECTORS

2.3.1 LINE VOLTAGE

The Model 7040 operates from either 115 V or 230 V, ± 10%, 50/60 Hz line source. A slide switch on the rear panel selects either of these line voltages. The switch has been preset at

the factory for the line voltage of the country to which the instrument is shipped. Normally this switch should not be touched unless the line voltage has been changed.

2.3.2 POWER ON-OFF SWITCH AND FUSE

AC power is applied through the POWER ON-OFF toggle switch mounted on the front panel. A panel light indicates when the Model 7040 is on. A fuse holder is located above the POWER switch. The correct value fuse for 115 VAC is 1 Amp Slo-Blo and for 230 V is 1/2 Amp Slo-Blo.

2.3.3 TRIGGER MODE SWITCH

This switch selects one of four major modes that triggers a delay cycle.

(1) MANUAL. A pushbutton provides one cycle of delay. Each depression of the MANUAL pushbutton starts a delay cycle. Delay data from the front panel or remote programming is strobed into the Model 7040 before the PRE-TRIGGER pulse and again at the start of the DELAYED PULSE.

(2) EXT TRIG. This mode is used when an external signal is used to trigger the Model 7040. There are two modes, A and B, and they differ as to when the updating of delay data occurs. In EXT TRIG A mode, the delay data is strobed in only at the start of the DELAYED PULSE. In EXT TRIG B mode, delay data is strobed in after the Model 7040 is externally triggered and again at the start of the DELAYED PULSE. Strobing occurs for approximately 150 ns. Data information can be changed 150 ns after the start of the strobe. Because of the extra strobe cycle, the INITIAL PULSE occurs approximately 250 ns after the external trigger in EXT TRIG B mode; in EXT TRIG A mode, the INITIAL PULSE occurs approximately 75 ns after the external trigger. See paragraph 2.2.3, part (1), for additional operating information.

(3) PERIOD. This mode converts the Model 7040 to a frequency synthesizer. There are nearly 100,000 discrete frequencies available from the Model 7040 from approximately 1 kHz - 5 MHz. These frequencies are equal to 1/(Delay + 200 ns). The units decade, 0 - 9 ns, does not contribute to the pulse period.

In the PERIOD mode, new delay cycles start 200 ns after the start of the DELAYED PULSE. Within that 200 ns, a data strobe occurs allowing delay data to be updated.

(4) INT. This mode provides four decade ranges as an internal trigger source. The trigger rate is continuously adjustable from 0.5 kHz to 5 MHz through the use of the four INT ranges and FINE vernier control. The FINE control provides more than a 10:1 control with overlap to the adjacent ranges. There is a ± 5 ns jitter between the Internal Trigger and the PRE-TRIGGER out. See paragraph 2.2.3, part (1), for additional information.

If trigger pulses in INT or EXT TRIG A modes occur before the end of the delay cycle, the next INITIAL PULSE starts about 200 ns after the start of the DELAYED PULSE. In EXT TRIG B mode, an external trigger pulse is inhibited until approximately 200 ns after the leading edge of the DELAYED PULSE.

2.3.4 EXT TRIG LEVEL AND SLOPE

The EXT TRIG LEVEL control determines the voltage level at which the Model 7040 will trigger. Triggering occurs when the input signal passes through a pre-determined level as set by this control. When the TRIGGER LEVEL control is set on the positive side of center, the generator will trigger on a more positive point of the input signal. When set on the negative side of center, the generator will trigger on a more negative point of the input signal.

The SLOPE switch determines whether the generator will trigger on a negative-going or a positive-going portion of the signal.

These controls operate in a manner similar to those found on oscilloscopes.

2.3.5 EXT TRIG CONNECTOR

A signal into this connector provides triggering in the EXT TRIG modes. The input impedance is 50 Ω, and input signals should not exceed ± 5 V (± 10 V max).

2.3.6 DELAY SWITCHES

The six DELAY switches determine the delay interval from 0 to 999,999 ns in nanosecond steps. The switches are arranged with the most significant digit on the left. The voltage on Pin 35 on the rear panel programming connector determines whether the front panel switches or remote levels control the delay. If the voltage is low, then the remote levels control; if the voltage is high, then the front panel switches control.

2.3.7 PRE-TRIGGER

This output provides a 10 ns wide pulse occurring 45 ns before the start of the INITIAL PULSE. One of its main functions is to trigger an oscilloscope so that the INITIAL PULSE may be seen.

2.3.8 INITIAL PULSE NEG CONNECTOR

This pulse is the start of the calibrated delay. The connector supplies a -1.8 V pulse from a 50Ω source or a -0.9 V pulse into a 50Ω load.

To obtain ECL logic levels with a 50Ω termination, connect a current source with about -30 mA to this connector which will give a -0.75 V offset. (Example: Connect 400 Ω to -12 V. Tie the other end of the 400Ω to this connector.) An inductance (in the μH range), in series with this offset resistor, helps to preserve the high frequency characteristics of the output pulse.

2.3.9 INITIAL PULSE POS CONNECTOR

This pulse is the start of the calibrated delay. It is coincident in time with the Initial Negative pulse. Its amplitude is adjustable from + 0.5 V to + 5 V into 50Ω.

2.3.10 INITIAL PULSE WIDTH AND INITIAL PULSE AMPLITUDE CONTROLS

The INITIAL PULSE WIDTH control determines the width of both the POSITIVE and the NEGATIVE INITIAL PULSES. The INITIAL PULSE AMPLITUDE controls the amplitude of only the POSITIVE INITIAL PULSE. The widths of both POSITIVE and NEGATIVE INITIAL PULSES

are identical and can be varied continuously from 15 ns to 1 μs. The amplitude of the POSITIVE INITIAL PULSE can be varied continuously from ± 0.5 V to + 5 V into a 50Ω load. The amplitude control is an attenuator designed to operate into 50Ω.

2.3.11 DELAYED PULSE POS, DELAYED PULSE NEG, DELAYED PULSE AMPLITUDE AND WIDTH

These connectors and controls function in the same way as their INITIAL PULSE counterparts. The DELAYED PULSE marks the end of the calibrated delay.

2.3.12 GATE

A +2.5 V signal into 50Ω is generated for a period of time equal to the DELAY setting with a maximum indeterminancy of 2 ns. With this output, the Model 7040 also functions as a programmable width generator.

---------- NOTE ----------

The GATE output will not function if the DELAYED PULSE is still present at the start of the next INITIAL PULSE.

2.3.13 GATED CLOCK

This connector provides, for the duration of the DELAY, a 100 MHz pulse train of +2 V into 50Ω. The number of clock pulses corresponds to the number formed by the five most significant delay digits, i.e., the number of 10 ns clock periods within the DELAY period.

2.3.14 J1, REAR CONNECTOR

This connector provides inputs for remote data lines. The DELAY inputs, the update input, and the EXT/INT input are DTL and TTL compatible. Figure 2-1 relates function to the corresponding pin number of J1. Delays are listed in nanoseconds.

FIG. 2-1

DELAY - ns	PIN #	DELAY - ns	PIN #	DELAY - ns	PIN #
1	1	2×10^2	6	4×10^4	27
2	2	4×10^2	23	8×10^4	28
4	19	8×10^2	24	1×10^5	11
8	20	1×10^3	7	2×10^5	12
1×10^1	3	2×10^3	8	4×10^5	29
2×10^1	4	4×10^3	25	8×10^5	30
4×10^1	21	8×10^3	26	Ground	36
8×10^1	22	1×10^4	9	Ext / Int	35
1×10^2	5	2×10^4	10	Update	18

(1) EXTERNAL/INTERNAL CONTROL. The level at Pin 35 determines whether the front panel switches or remote levels control the delay. The signal at Pin 35 enters a DTL gate. A low level ($\leq$ + 0.5 V) or short circuit corresponds to remote level control; a high level ($\geq$ 2.5 V) or open circuit corresponds to front panel control.

(2) DELAY DATA INPUTS. The delay data is entered in an 8-4-2-1 BCD code. The inputs are DTL gates, and the logic levels are identical to those for the EXTERNAL/INTERNAL control. A high level corresponds to a "1", i.e., positive logic. The delay data should be present at J1 for 200 ns before and after the start of the data strobe. In PERIOD, EXT TRIG A, and INT modes the strobe starts at the leading edge of the DELAYED PULSE. In the EXT TRIG B mode, data strobe occurs at both the time of external triggering and at the leading edge of the DELAYED PULSE.

(3) UPDATE. A high level at the update input allows new delay data to be strobed into the Model 7040. A low level, open or short circuit at Pin 18 has no effect. Delay data should be present at the data inputs 200 ns preceding the start of update. An update signal also stops any delay cycle in progress and prepares the Model 7040 for the start of another cycle. Operation is inhibited for the duration of the update signal or 1 μs, whichever is longer.

SECTION 3
THEORY OF OPERATION

3.1 INTRODUCTION

This section of the manual contains a description of the circuitry in the Model 7040 Programmable Digital Delay Generator. A complete block diagram, Figure 3-3 (located at the end of this section), shows the overall relationship of the various circuits. A description of the block diagram is given below in paragraph 3.2. Detailed circuit description is given below in paragraph 3.3.

3.2 BLOCK DIAGRAM

3.2.1 GENERAL

The precise delays of the Model 7040 are generated by a counter that counts from an initial, preset value to a final value. The preset value of the counter is determined either by front panel controls or remote logic levels. A 100 MHz crystal-controlled clock for the counter insures an accurate delay. The enabling signals for the counter come from one of three sources: an external trigger, an internal rep rate generator, or an internally generated reset signal. A main gate, the source of the enabling signal for the counter, also indirectly initiates a pretrigger, an initial pulse, a gate output, and a gated clock. An end-of-count signal stops the gated clock and the gate output and starts the delayed pulse out. The end-of-count signal also starts a reset sequence which prepares the Model 7040 for another delay cycle.

3.2.2 EXTERNAL TRIGGER BUFFER

The External Trigger Buffer serves as a buffer from the EXT TRIG connector to the Trigger Input Discriminator. The External Trigger Buffer functions only when the TRIGGER MODE switch is in either EXT TRIG A or EXT TRIG B modes.

3.2.3 TRIGGER INPUT DISCRIMINATOR

The Trigger Input Discriminator allows the EXT TRIG LEVEL potentiometer and the SLOPE toggle switch to control the point of triggering. The output of the Trigger Input Discriminator goes either to the Tunnel Diode Lockout or the B Mode Lockout, and the TRIGGER MODE switch determines the path taken.

3.2.4 B MODE LOCKOUT

The purpose of the B Mode Lockout is to prevent the signal from the Trigger Input Discriminator from arriving at the B Mode One-Shot when the Main Gate Latch (to be discussed later) indicates that the Counter is counting up, i.e., the end-of-count has not been reached. This prevents external triggers from resetting the Counter during counting.

3.2.5 B MODE ONE-SHOT

When the TRIGGER MODE switch is in the EXT TRIG B position, the output of the Trigger Input Discriminator is routed to the B Mode One-Shot (provided there is no B Mode Lockout). The B Mode One-Shot immediately produces a signal for a Reset Generator and, after a fixed time delay, presents a signal to a Tunnel Diode Lockout.

3.2.6 UPDATE ONE-SHOT

The Update One-Shot allows the changing of the programmed delay at any given time. The output of the Update One-Shot goes via the B Mode One-Shot into the Reset Generator and Tunnel Diode Lockout.

3.2.7 MANUAL TRIGGER SHAPER

The Manual Trigger Shaper is a latch controlled by the MANUAL pushbutton. It triggers the B Mode One-Shot.

3.2.8 RESET GENERATOR

Triggering of the Reset Generator by the B Mode One-Shot leads to the production of a reset signal. This reset signal allows a new programmed delay to be strobed into the Counter Preset. Further discussion on the Reset Generator follows in paragraph 3.2.29.

3.2.9 TUNNEL DIODE LOCKOUT

The Tunnel Diode Lockout prevents triggering of a new delay cycle until a lockout reset signal is received. There are three sources to start lockout: 1) in the EXT TRIG A mode, from the Trigger Input Discriminator, 2) in the EXT TRIG B mode, from the B Mode One-Shot and 3) in the INT mode from the Internal Rep Rate Generator. Once a lockout signal is received, further signals from any of these sources will not retrigger the Tunnel Diode Lockout until a lockout reset has been received. The lockout reset signal comes from the Pretrigger Amplifier. In the PERIOD mode, the Tunnel Diode Lockout is always in the start lockout mode. The Tunnel Diode Lockout signal enables a Reclocked Trigger.

3.2.10 INTERNAL REP RATE GENERATOR

The Internal Rep Rate Generator serves as a variable frequency trigger source. The trigger frequency is controlled by the INT positions of the TRIGGER MODE switch and the FINE frequency potentiometer.

3.2.11 100 MHz OSCILLATOR

The 100 MHz Oscillator is crystal-controlled and serves as a system clock. Many of the circuit blocks are synchronized to this clock to preserve an accurate relationship between the various timing signals in the Model 7040. This oscillator also serves as the clock for the counter and hence determines the accuracy and stability of the digital delay. The oscillator outputs, Ø1 and Ø2, are nearly 180^{o} out of phase.

3.2.12 RECLOCKED TRIGGER

The Reclocked Trigger is a bi-stable circuit that presents an enable signal to the Main Gate. The leading edge of the output from the Reclocked Trigger is synchronized to Ø2; thus the term "reclocked". The state of the Reclocked Trigger is returned to its initial condition by the output of the Reset Generator. Only then can it re-enable the Main Gate. In the PERIOD mode, with the Tunnel Diode Lockout in the lockout state, the Reclocked Trigger changes states at reset and at the Ø2 signal following reset.

3.2.13 MAIN GATE

The Main Gate is reclocked with Ø1 and sets the Main Gate Latch.

3.2.14 MAIN GATE LATCH

The output of the Main Gate Latch enables the Counter, End-of-Count Latch, and Initial Pulse Latch. This latch is reset by the Reset signal.

3.2.15 INITIAL PULSE LATCH

The Initial Pulse Latch is set by Ø2 to enable the Reclocked Initial Gate and drive the Pretrigger Amplifier. It is reset by the Reset signal.

3.2.16 PRETRIGGER AMPLIFIER

The Pretrigger Amplifier differentiates and amplifies the leading edge of the Initial Pulse Latch to reset the Tunnel Diode Lockout. It also presents a pretrigger signal at the PRETRIGGER connector.

3.2.17 RECLOCKED INITIAL GATE

The Reclocked Initial Gate receives an output signal from the Initial Pulse Latch. This gate is synchronized with Ø1 and sets both the Gated Clock Latch and the Initial Pulse Width Latch.

3.2.18 INITIAL PULSE WIDTH LATCH

The Initial Pulse Width Latch is set by the signal from the Reclocked Initial Gate and is reset by the width control circuit. The INITIAL PULSE WIDTH potentiometer controls this reset time. The output of the Initial Pulse Width Latch then proceeds into the Initial Pulse Amplifiers. Another output of the Initial Pulse Width Latch sets the Gate Latch.

3.2.19 INITIAL PULSE AMPLIFIERS

The Initial Pulse Amplifiers amplify the signal from the Initial Pulse Width Latch and present positive and negative outputs at the INITIAL PULSE POS connector and INITIAL PULSE NEG connector. The INITIAL PULSE AMPLITUDE potentiometer controls the amplitude of the positive pulse out.

3.2.20 COUNTER

The Main Gate Latch also enables the Counter to count up from a preset level to a final value. The clock for the Counter is Ø2.

3.2.21 COUNTER PRESET

The Counter Preset is comprised of logic that allows the Counter to be preset to an initial value.

3.2.22 COUNTER PRESET BUFFER

The Counter Preset Buffer determines whether remote logic levels or the front panel DELAY control settings enter the Counter Preset. An external/internal control level into the Counter Preset Buffer determines this. Information from the Counter Preset Buffer is strobed into the Counter during reset.

3.2.23 END-OF-COUNT GATE

The End-of-Count Gate presents a signal to the End-of-Count Latch when the Counter has reached its final value.

3.2.24 END-OF-COUNT LATCH

The End-of-Count Latch was enabled at the start of the count cycle by the Main Gate Latch. At the end of the count cycle, the End-of-Count Gate sets the End-of-Count Latch. The reset signal resets the End-of-Count Latch.

3.2.25 RECLOCKED DELAYED GATE

The End-of-Count Latch signal is synchronized with Ø1 at the Reclocked Delayed Gate. The Reclocked Delayed Gate signal then proceeds to stop the Gated Clock Latch, enable the Reset Generator and drive the Programmed Delay Lines. The Reclocked Delayed Gate is reset by the reset signal.

3.2.26 GATED CLOCK LATCH

The Gated Clock Latch was set by the Reclocked Initial Gate and is now reset by the Reclocked Delayed Gate. The duration of the set period of the Gated Clock Latch is equal to the counting period.

3.2.27 GATED CLOCK GATE

The signal from the Gated Clock Latch enables Ø2 to be transmitted through the Gated Clock Gate to the Gated Clock Amplifier. Ø2 is also inverted by the Gated Clock Gate and is used by the Reset Counter as a clock, Ø3.

3.2.28 GATED CLOCK AMPLIFIER

The Gated Clock Amplifier amplifies the signal from the Gated Clock Gate. The signal is presented at the GATED CLOCK connector.

3.2.29 RESET GENERATOR

The Reset Generator is a latch whose state is set by either the Reclocked Delayed Gate or the B Mode One-Shot. The setting of this latch is transmitted through buffers to produce the reset signal.

3.2.30 RESET COUNTER

The set state of the Reset Generator acts as an enabling signal to a Reset Counter. When the Reset Counter has counted to a final number, it resets the Reset Generator. Here the Reset Counter acts as an internal delay generator and controls the width of the reset pulse.

3.2.31 RESET BUFFER

The Reset Buffer acts as a buffer between the Reset Generator and the circuits that are reset.

3.2.32 PROGRAMMED DELAY LINE

The Programmed Delay Line is inserted in the delay sequence to obtain delays from 0 through 9 ns. The 100 MHz Oscillator and the Counter provide delays in multiples of tens of nanoseconds.

3.2.33 PROGRAMMED DELAY LINE BUFFER

This buffer selects whether the units decade of the front panel DELAY settings or the units decade of the remote programmed delay is used. The same external/internal logic control signal that controls the Counter Preset Buffer controls the Programmed Delay Line Buffer. This delayed signal then proceeds to the Delayed Pulse Width Latch.

3.2.34 DELAYED PULSE WIDTH LATCH

The Delayed Pulse Width Latch is set by the signal from the Programmed Delay Lines, and is reset by the width control circuit. The DELAYED PULSE WIDTH potentiometer controls this reset time. The output of the Delayed Pulse Width Latch then proceeds into the Delayed Pulse Amplifiers. The Delayed Pulse Width Latch also sends a reset signal to the Gate Latch.

3.2.35 DELAYED PULSE AMPLIFIERS

The Delayed Pulse Amplifiers amplify the signal from the Delayed Pulse Width Latch and present positive and negative signals at the DELAYED PULSE POS connector and DELAYED PULSE NEG connector. The DELAYED PULSE AMPLITUDE potentiometer controls the amplitude of the positive pulse out.

3.2.36 GATE LATCH

The Gate Latch is set by the Initial Pulse Width Latch and reset by the Delayed Pulse Width Latch. The Gate Latch width represents the actual delay time.

3.2.37 GATE AMPLIFIER

This Gate Latch signal is then amplified and presented at the GATE connector.

3.3 CIRCUIT DESCRIPTION

3.3.1 EXTERNAL TRIGGER BUFFER AND TRIGGER INPUT DISCRIMINATOR

(Refer to Schematic 7040-13 in Section 5.)

The External Trigger Buffer is comprised of D5 and Q6. The signal present at the EXT TRIG input is fed to the emitter of Q6. Diode D6 or D7 connects emitter resistor R42 to a -5.2 V supply through the TRIGGER MODE switch in only the EXT TRIG A and EXT TRIG B modes. Q6 operates only in these two modes.

The signal at the emitter of Q6 then enters the Trigger Input Discriminator, which uses a tunnel diode to provide fast switching. Changes in the state of tunnel diode TD1 are sensed as current changes in transformer T1 and transmitted to the base of either Q9 or Q13. Slope control for the Trigger Input Discriminator is provided by toggle switch S2 and transistors Q7 and Q8.

In the positive slope position (as shown in the schematic), Q8 is saturated. Potentiometer R47 sets the level at one node of a resistance bridge, R43 through R46. The other node, at the emitter of Q6, is the input of the Trigger Input Discriminator. As a signal from Q6 goes positive, through threshold, tunnel diode TD1 (D8) switches to its high voltage state. The current through T1 increases since the voltage across R54 and R53 increases. Note that TD1 changes to its high voltage state as the voltage at the emitter of Q6 moved with a positive slope.

For a negative slope, Q7 is saturated with the anode of TD1 held close to ground. Now TD1 is switched to its high voltage state when the signal from the emitter of Q6 moves negatively through threshold.

Again the current in transformer T1 is increased. Transformer T1, an AC coupler and differentiator, is needed because of the changing node voltages with changing level control.

Increases in T1 current will turn Q9 or Q13 on harder. Either Q10 or Q12 will be saturated by the TRIGGER MODE switch to cause only Q9 or Q13 to conduct more. For example, in EXT TRIG A mode, the base of Q12 is held below ground by voltage divider R61, R62. The base of Q10 is connected to the +6 V supply through R56. Thus Q10 is saturated and Q12 is off. With Q10 saturated, Q9 will not experience any fluctuations at its base. The increase in current in T1 then turns off D10 to move the emitter of Q13 positive. In EXT TRIG B mode, Q12 is saturated and Q10 is turned off. As T1 turns on Q9, a positive spike is presented to the base of emitter follower Q11. The signal from the collector of Q9 is then sent to the B Mode Lockout.

3.3.2 B MODE ONE-SHOT, B MODE LOCKOUT, UPDATE ONE-SHOT, and MANUAL TRIGGER SHAPER

(Refer to Schematic 7040-13 in Section 5.)

The B Mode Lockout is comprised of transistors Q25 and Q26. If either the base of Q25 or the base of Q26 is low, the increasing current from Q9 will be clamped by Q25 or Q26 at the base of Q11. The input to the base of Q25 comes from the Reclocked Main Gate Latch which prevents the generation of a B Mode pulse between the start of the delay cycle and the occurrence of the reset pulse. The base of Q26 goes to an inverted reset pulse that clamps Q9 during reset.

When the B Mode Lockout is not preventing it, the positive spike from Q11 is transmitted to Pin 1 of IC2, the B Mode One-Shot. The positive spike at Pin 1 of IC2, a dual four-input ECL gate, results in a positive-going signal at Pin 6 of IC2 that sets the Reset Generator via R226 to start a reset cycle. At the same time, Pin 5 of IC2 moves to a low level state to begin the one-shot period. At the end of the one-shot period, Pin 5 moves positively and injects current into R11 for a short period of time. This differentiated edge results in a positive spike at the collector of Q1. This is transmitted via diode D3 to the Tunnel Diode Lockout.

To understand the operation of the B Mode One-Shot, assume that Pin 5 is high and Pin 6 is low (stable state). The high level at Pins 5 and 10 results in a low level at Pin 9. In this steady state condition, Pin 11 is low. Thus, we have a fixed voltage across C2. Note that inputs 1, 2, 3 and 4 are low confirming our original assumption about the steady state.

The positive spike from Q11 takes Pin 10 low. The charge on C2 makes Pin 11 lower than Pin 10 thus causing Pin 9 to go positive. The high level at Pin 9 keeps Pin 5 low as C2 is charged through R6. When Pin 11 reaches a sufficiently positive level, Pin 9 will become low, switching Pin 5 to a high level and thus changing the one-shot back to its stable state.

IC1 is a manual trigger shaper connected as an RS flip-flop. The RS flip-flop keeps the contact bounces of the MANUAL pushbutton switch from spuriously triggering the B Mode One-Shot. Depressing the MANUAL pushbutton results in a positive leading edge that is differentiated by C1 and coupled to Pin 2 of the B Mode One-Shot to start a delay cycle.

The Update One-Shot is comprised of IC3, a monolithic monostable multivibrator, and a buffer transistor, Q2. The positive-going signal at J1 Pin 18 will produce a pulse at Pin 6 of IC3 that is approximately 1 μs wide. This signal is differentiated by C4 and sent to Pin 3 of IC2, the B Mode One-Shot, to begin reset and allow new data to be strobed into the Counter.

3.3.3 TUNNEL DIODE LOCKOUT and INTERNAL REP RATE GENERATOR

(Refer to Schematic 7040-13 in Section 5.)

Tunnel diode TD2 (D12) together with Q14, Q15 and Q16 comprise the Tunnel Diode Lockout. To set the lockout state, a positive spike is received from Q13 in EXT TRIG A; from Q1 of the B Mode One-Shot; or from Q21 of the Internal Rep Rate Generator. The base of Q14 is controlled through resistor divider R65, R66 by the collector of Q2. Q14 prevents the setting and causes resetting of the lockout state during the quasi-stable state of the Update One-Shot or during the presence of an update signal at J1 Pin 18. The collector of Q2, the drive signal for the base of Q14, is wired OR'ed to Pin 1 of the Update One-Shot. When the collector of Q2 is low, Q14 prevents any incoming signal from setting the Tunnel Diode Lockout.

In the PERIOD mode, Q15 is turned on via R68 and the TRIGGER MODE switch. With Q15 on, TD2 is kept in its high voltage state through R71, and the Tunnel Diode Lockout is continually in this set mode. In all modes, the Tunnel Diode Lockout is reset by a short pulse from Q24 that takes TD2 to its low voltage state.

The signal at the anode of TD2 is sent through buffering diode D13 to determine the emitter level of Q16. A high level at the emitter of Q16 enables the Reclocked Trigger.

Q19 and Q20 form a variable frequency astable multivibrator with Q21 serving as a buffer and level translator. Q19 and Q20 operate only during the INT modes since their common emitter resistors, R85 and R84, are connected via the mode switch to a -5.2 V supply only in INT modes. The frequency range is determined by capacitors C23 - C26; the FINE frequency is controlled by potentiometer R91. L3 and R87 differentiate the waveforms into Q21. D11 allows only the positive-going spike from Q21 to enter the Tunnel Diode Lockout.

To understand the operation of the Internal Rep Rate Generator, assume that Q19 is on and Q20 off. In order to turn Q20 on, the base of Q20 must rise above ground. The rate at which the base of Q20 moves positively is determined by the value of the capacitor selected and the position of the FINE control potentiometer. When Q20 turns on and Q19 turns off, the collector of Q19 moves positively and hence moves the base of Q20 more positively. This regenerative action tends to turn Q20 on harder and hence turns Q19 off harder. With Q19 completely off, the base of Q20 is moved positively since the voltage across the range capacitor cannot change instantaneously. The base of Q20 now moves negatively at a rate determined by the value of the range capacitor and the position of the FINE frequency potentiometer. When the base of Q20 has moved sufficiently negative to start turning Q20 off, Q19 will start to conduct, moving the base of Q20 even lower through the range capacitor. In the end, Q19 will be fully conducting and Q20 will be fully off to start a new timing cycle.

3.3.4 100 MHz OSCILLATOR

(Refer to Schematic 7040-13 in Section 5.)

The oscillator consists of IC4 and a 100 MHz crystal. One end of the crystal is connected to Pin 6, an input, and the other end to Pin 3, the inverted output. The signal fed back to the non-input end of the crystal tends to increase the voltage across the crystal. Trimmer C9 serves as a phase shift control, and trimmer C8 serves as a frequency adjust. R20 helps to bias Pin 6 near threshold. Resistors R23 - R26 help to backmatch the Ø1 and Ø2 output lines.

3.3.5 RECLOCKED TRIGGER, MAIN GATE, MAIN GATE LATCH

(Refer to Schematic 7040-13 in Section 5.)

The Reclocked Trigger, consisting of TD3 (D14), has been enabled by the emitter of Q16 moving positively. A positive-going waveform from Ø2 is differentiated by C11 and causes TD3 to switch to its high voltage state; thus the term "reclocked". The Reclocked Trigger remains in this state until a positive signal at the base of Q17 during reset changes TD3 to its low voltage state. Q18 serves as an emitter supply for R80, and the level is such that Q17 is cut off when a low level is present at its base.

The high level state of TD3 goes through R28 to the base of Q3, part of the Main Gate circuitry. This level is inverted by Q4 and appears as a low level at Pin 2 of IC5, also part of the Main Gate. When Ø1 goes low, Pin 6 will move high. This reclocked signal causes Pin 13 to be high and Pin 8 to be low. The Pin 13 to Pin 11 connection makes this gate in IC5 a latch. The enabling state of the Main Gate Latch is with Pin 8 low.

This latch is reset via D4 when the base of Q5 goes negative, causing the emitter of Q5 to go negative and Pin 13 of IC5 to go low. The drive for D4 comes from the reset circuitry through an inverter which is part of IC6. Note that part of IC5 gates the clock, and the remaining gate in IC5 is a latch.

3.3.6 INITIAL PULSE CIRCUITRY and PRE-TRIGGER AMPLIFIER

(Refer to Schematic 7040-15 in Section 5.)

One of the outputs on the Main Gate enters IC64, the Initial Pulse Latch. IC64 is a type D flip-flop with two clock inputs. With one of the clock controls, the Main Gate, going low, IC64 is set on the next positive excursion at Pin 8. With Q connected to S, the flip-flop remains in a set condition until a reset pulse enters. R-S operation predominates over clocked operation.

One of the outputs of IC64 is transmitted to the base of Q22, the input of the Pre-Trigger Amplifier. The edges are differentiated by L4 and R94 in the Pre-Trigger Amplifier and presented to the PRE-TRIGGER connector via Q23. D15 allows only positive pulses to enter this connector. This positive pulse also causes Q24 to reset the Tunnel Diode Lockout. Another output of the Initial Pulse Latch goes to the aforementioned B Mode Lockout.

With the setting of the Initial Pulse Latch, Pin 3 goes negative. This is transmitted via DL1, a 15 ns delay line, to one of the inputs of IC65, a part of the Reclocked Initial Gate. DL1 helps to establish the fixed delay between the PRE-TRIGGER output and the leading edge of the INITIAL PULSE. DL1 makes this fixed delay less dependent on the propagation delays of the circuitry.

The Reclocked Initial Gate is comprised of IC66 and part of IC65. Pin 6 of IC66 is high and Pin 8 of IC66 is low after a positive reset at Pin 10. Before the setting of the Initial Pulse Latch, Pin 6 of IC65 was held low by the output of the Initial Pulse Latch. With both Pins 4 and 5 of IC66 low, Pin 6 will have a high output and Pin 8 a low output. This is a stable state previous to setting of the Initial Pulse Latch. When the Initial Pulse Latch is set, Pin 2 of IC65 will move low allowing Pin 6 of IC65 to move high when Ø1 at Pin 3 of IC65 moves low. This, in turn, causes Pin 6 of IC66 to move low and Pin 8 of IC66 to move high. The high level of Pin 8 of IC66 is transmitted to one of the inputs of IC65 changing Pin 6 of IC65 back to its low state. IC65 has thus produced a narrow positive pulse at Pin 6. IC66, however, is latched into a set position and is reset after the delay cycle has been completed. The output from Pin 6 of IC65 then proceeds to set the Gated Clock Latch, IC63, and the Initial Pulse Width Latch, IC67.

The positive pulse from IC65 passes through a 5 ns delay line, DL2. The function of DL2 is the same as DL1 in that it helps to establish a fixed delay between the PRE-TRIGGER and the INITIAL PULSE and at the same time makes the dependency on propagation delays minimal. The effect of R185, DL2 and C50 is to control when the threshold at Pin 2 of IC67 is crossed by integrating the signal from Pin 6 of IC65. C50 is used to adjust the coincidence between the INITIAL PULSE and DELAYED PULSE at zero delay.

The positive-going waveform at Pin 2 of IC67 causes Pin 1 to go positive and Pin 6 to go negative. The positive-going Pin 1 of IC67 turns on Q52, part of an emitter coupled current mode pair in the negative amplifier. The other half of the current pair, Q53, turns off and its collector moves positive turning off Q54. When Q54 turns off, the level at the INITIAL PULSE NEG connector goes to a level determined by voltage divider R211, R212, and the load. When IC67 is reset by the width control circuit, Q53 will turn on causing Q54 to turn on. When Q54 turns on, the collector of Q54 will return to a base line near ground. R213 acts as a threshold control to adjust the coincidence between the edges of the negative and positive pulses.

Diode D77 clamps the positive excursion at the collector of Q53. Diode D76 clamps the emitter of Q54 and insures that both Q54 and Q53 operate in non-saturating modes. When the collector of Q54 is near ground, its emitter is still at +0.7 V; when Q53 is on, its collector is near ground while its emitter is at roughly -1.4 V. The output of Pin 1 of IC67 goes via differentiator C51 to Pin 11 of IC62, the Gate Latch.

When Pin 9 of IC67 goes negative (Pin 12 of IC67 is already negative), Pin 8 of IC67 will go positive, causing Pin 6 to remain low in this latched condition.

The negative-going output from Pin 13 of IC67 is then sent to the base of Q45, part of the positive pulse amplifier. This negative-going level is translated to the base of Q46 forcing Q46 off and Q47 on. The base current for Q47 comes from ground through C52. With Q46 turned off, the emitter of emitter follower Q49 will move positively and present a positive pulse at the INITIAL PULSE POS connector.

The AMPLITUDE control is a ganged potentiometer that is part of the bridged T attenuator. In the maximum amplitude position, R201A is a short and R201B is 500 Ω. In the minimum amplitude position, R201A is 500Ω and R201B is a short. In the former case, the signal passes straight through the attenuator, and in the latter case, R201A forms a voltage divider with an equivalent resistor of R200 and the load resistor in parallel.

When the pulse is not present, Q48 and Q47 act as a baseline restorer. For example, if the baseline should go negative, Q48 will turn on harder thus turning on Q47 harder. Q46 will, therefore, conduct less current causing the base of Q49 to go more positive. This results in a restoration of the baseline. D73 and D74 limit the excursion of the voltage across C52 during turn on of the Model 7040.

Q50, Q51, and R205 provide the width control circuit that is used to reset the Initial Pulse Width Latch. The positive pulse at the base of Q50 turns off Q50 and allows C56 to charge positively through R202. The base of Q51 is controlled by the WIDTH potentiometer. When the emitter of Q51 reaches a point that is nearly one diode drop above the base of Q51, Q51 turns on to produce a positive-going waveform at Pin 12 of IC67 that resets the Initial Pulse Width Latch. The positive waveform at Pin 12 of IC67 will cause Pin 8 to go negative resulting in low inputs at both Pins 2 and 5 of IC67. Pin 6 now moves positive to complete this steady-state condition. This turns on Q46 and marks the end of the INITIAL PULSE. Q50 now turns on to discharge C56, and the Initial Pulse Width circuitry is ready to produce another INITIAL PULSE.

3.3.7 COUNTER, COUNTER PRESET, COUNTER PRESET BUFFER, and END-OF-COUNT GATE

(Refer to Schematic 7040-14 in Section 5.)

The output from the Main Gate Latch also enters the Counter at Pin 6 of IC23. Basically, the Counter is a five-decade, binary-coded decimal counter. The initial value of the Counter is preset when data is strobed in by the reset signal. The source of this data is either the front panel DELAY controls or the remote programming delay inputs. The initial value of the Counter is the nines complement of the desired delay. When the Counter reaches the final value of 99999, it sends a signal to the End-of-Count Latch via the End-of-Count Gate.

In explaining the need for setting the initial count of the Counter to the nines complement of the desired delay, we will use binary coded decimal numbers. The convention adhered to in this manual will be that the least significant bit is on the right end of a number, e.g., 1000 is 8 and not 1. The nines complement of a number is that number subtracted from 9. In the case of an 8-4-2-1 BCD code such as used here, the nines complement of a number is that number subtracted from 1001. When the nines complement of the programmed delay is set into the counter as an initial value, the counter starts at that number and counts up to 99999 at which point an end-of-count signal is generated. The conversion of the input data to nines complement is necessary because the counter counts up, not down.

With the front panel DELAY controls, the nines complement is coded by the front panel switches. See Figure 3-1 below.

FIG. 3-1

	BCD NUMBER				9's COMPLEMENT			
DEC. NO.	Q_4 8	Q_3 4	Q_2 2	Q_1 1	Q_4' 8'	Q_3' 4'	Q_2' 2'	Q_1' 1'
0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	0
2	0	0	1	0	0	1	1	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	0	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	0	1	0
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	0	0

The remote programmed BCD inputs must be converted to the nines complement before it is presented to the Counter. To explain this encoding, we will use as an example the least significant counter decade. For all the remaining decades, the remote programming inputs are encoded in exactly the same fashion. Refer to the above figure when necessary.

By looking at Figure 3-1, we can determine the relationship between each bit of the nines complement and one or more of the BCD bits. Note that Q_1' is a complement of Q_1 for all decimal numbers so $Q_1' = \overline{Q}_1$. Also note that the second bit in the nines complement number is always equal to the second bit in its corresponding BCD number for all decimal numbers. So, $Q_2' = Q_2$. Notice that the third bit of the nines complement number is equal to one when the second bit of the BCD number is one and the third bit of the same BCD number is zero, or when the second bit of the BCD number is zero and the third bit is one. When the second and third bits of the BCD number are both zeros or both ones, the third bit of the nines complement is zero. This can be written as

$$Q_3' = Q_2 \cdot \overline{Q}_3 + \overline{Q}_2 \cdot Q_3 = Q2 \oplus Q3.$$

The fourth bit of the nines complement is only equal to one when the second, third and fourth bits of the BCD number are equal to zero.

$$\text{Thus, } Q_4' = \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{Q}_4.$$

As an example, let us assume that the number six is programmed into the least significant decade. The 0110 code present at the input should preset the least significant decimal counting unit to 0011. The low level at Pin 3 of J1 is passed through two inverters and appears at Pin 8 of IC11 as a low level. This keeps node 53 low and makes Pin 1 of IC22 high.

During reset, Pin 3 of IC6 moves high causing Pins 6 and 3 of IC1 to present a low signal at Pins 5 and 2 of IC22. This low signal is present for the duration of the reset pulse and is a data strobe signal. With Pins 4 and 5 of IC22 low, Pin 6 will move high to set IC23. Since Pin 1 of IC22 is high, a negative-going strobe signal has no effect on the already low output at Pin 3. Thus, S = 1 and R = 0, and IC23 is set at Q = 1.

The Q2 = 1 signal at Pin 4 of J1 is inverted by IC11 and results in the low level at node 52. As with IC23, this low level at node 52 sets IC24 during reset.

The high levels at Pins 4 and 21 of J1 are Exclusive-OR'ed by IC12 and result in a low level at Pin 8 of IC12. This is inverted by IC11 and results in a high level at node 51. This positive level keeps Pin 8 of IC25 low and results in a low level at Pin 11 of IC21. During reset, Pin 12 of IC26 is now made high while Pin 2 remains low (R = 1, S = 0). This resets IC26, and the state of IC26 is Q = 0.

The second, third and fourth bit inputs at Pins 4, 21 and 22 of J1, respectively, are inverted and serve as inputs to IC13. The high level at Pin 4 or 21 results in a low level at Pins 10 and 11 of IC13 to make Pin 8 of IC13 high. The high level at node 50 results in a resetting of IC27 during reset to make the state of IC27 Q = 0.

Thus, the BCD number 0110 has preset the least significant decimal counting unit to 0011. One may have noted that IC11 - IC13 provide the inverse of the above encoding equations. Another inversion occurs at the gate connected to the set inputs of the flip-flops.

The signal at Pin 35 of J1 controls whether the front panel DELAY controls or the remote programming inputs determine the data preset into the Counter. High level or open circuit at Pin 35 corresponds to front panel control; a low level or a short to ground at Pin 35 indicates remote programming control.

For remote programming, the input at Pin 35 of J1 is near ground and, after passing through two inverters, causes Q1 to saturate. The collector of Q1 provides the power supply for input encoders IC11 - IC18. With Q1 saturated Q2 is off, thus reverse biasing diodes D41 - D60. The cathode of D20 is one diode drop below ground. Positive levels from the encoding gates to any of resistors R115 - R134 will turn on the corresponding diodes D21 - D40. A low level from these gates will result in back biasing the corresponding diodes.

With a +5 volt signal or an open circuit at Pin 35, a high level will be present at the base of Q1 to turn off Q1 and turn on Q2. The supply to IC11 - IC18 is turned off with Q1. Q2 saturates to place the anodes of diodes D41 - D60 near ground and to provide a current path for diodes D21 - D40.

When a negative-going signal from the Main Gate Latch enters Pin 6 of IC23, a type D flip-flop, it allows positive-going signals from Ø2 into Pin 8 to clock the flip-flop. The D input at Pin 10 is connected to the $\overline{Q}$ output at Pin 3, and under these conditions the flip-flop changes state with each clock pulse. Since the RS inputs are made low by the high level at Pin 6 and Pin 3 of IC1 (except during reset), the counter begins to count up. The discussion here will deal with the least significant decimal counting unit operation which is similar to all subsequent decimal counting units.

Thus far we have IC23 changing state with each clock pulse. By using the BCD numbers in Figure 3-1 as the count sequence, one can note that IC24, Q_2, changes state when IC23, Q_1, is in a high state and a clock pulse is present. When the nine count is reached, IC24 must be prevented from changing state at the next clock pulse. When IC23 changes from the one state to the zero state, $\overline{Q}_1$ moves positively and serves as a clock signal for IC24, Q_2. Q_2 will only change state with this clock pulse while IC27, Q_4, is zero. When Q_4 equals one, this input at $\overline{J}$, Pin 3 of IC24, insures that the state of IC24 is $Q = 0$ ($\overline{J} = 1$, $\overline{K} = 0$, $\overline{C}_D = 1$).

Also from Figure 3-1, note that IC26, Q_3, changes state only when Q_2 moves from one to zero. This is implemented by using $\overline{Q}_2$ as a clock input for Q_3.

IC27, Q_4, changes from zero to one when the previous state is Q_1, Q_2, and Q_3 all equal to one. Note that the clock pulse first changes Q_1 which, in turn, changes Q_2 and, in turn, changes Q_3. Q_4 changes state when inputs to Pin 5 and Pin 3 of IC27 indicate that $\overline{Q}_2$ and $\overline{Q}_3$ equal 0, and the positive-going signal from $\overline{Q}_1$ indicates that Q_1 is moving from $Q = 1$ to $Q = 0$ ($\overline{J} = \overline{K} = 0$, $\overline{C}_D = 1$). Here we are taking advantage of the finite propagation delay in Q_2 in that Q_2 does not switch immediately with the clock pulse from $\overline{Q}_1$ but stays in the $Q_2 = 1$ position long enough to enable Q_4 to change. Note that Q_4 will move from one to zero when Q_2 and Q_3 are zero and when Q_1 moves from one to zero ($\overline{J} = 1$, $\overline{K} = 0$, $\overline{C}_D = 1$).

When the least significant DCU switches from 9 back to zero, it generates a clock pulse for the next DCU. $\overline{Q}_4$ acts as a clock for the next DCU. The positive-going signal at $\overline{Q}_4$ indicates that the first DCU is changing from a nines count back to a zero count. When the second DCU switches from a nines count to a zero count, it triggers the third DCU and so on.

The End-of-Count Gate is comprised of IC56, IC57 and IC58. The End-of-Count Gate detects when the Counter has reached a final value. This results in a low level at Pin 13 of IC56 when the 99999 count is reached. IC58 detects the state of the most significant flip-flop and has a low output when the first flip-flop, IC51, is high or its $\overline{Q}$ is low, when the second flip-flop, IC52, is in the $Q = 0$ state, and when IC55, the fourth flip-flop, is in the $Q = 1$ state or when its $\overline{Q} = 0$. These conditions occur only during a 9. The output at Pin 8 of IC57 is low only when the fourth and fifth decades are at a nines count. This decoding scheme continues to Pin 13 of IC56 which is low only when all the decades are at nines. Although the Counter is a serial counter, propagation delay effects are minimized by the higher significant decades reaching their final value before the least significant decade reaches its final value. The output at Pin 13 of IC56 moves positive at the first clock pulse after the all nines state.

3.3.8 END-OF-COUNT LATCH, RECLOCKED DELAYED GATE, RESET GENERATOR, RESET BUFFER and RESET COUNTER

(Refer to Schematic 7040-16 in Section 5.)

The output from the End-of-Count Gate enters the End-of-Count Latch at Pin 3 of IC70. Pin 4 of IC70 has been made low by the output of the Main Gate Latch. When Pin 3 of IC70 moves from a negative level to a positive level, this transition sets IC70 ($\overline{J}_D = 1$, $\overline{K}_D = 0$).

When IC70 is set, Pin 1 will move negatively allowing the output of the Reclocked Delayed Gate, Pin 8 of IC71, to move positively when

Ø1 moves negatively. The output of the Reclocked Delayed Gate goes to Pin 12 of IC63 to reset the Gated Clock Latch. This output is AC coupled via C65 to the base of Q65 and sets the Reset Generator via Pin 11 of IC66.

The Reset Generator is comprised of part of IC66 and part of IC71 connected as an RS flip-flop. The reset cycle is started either by Pin 8 of the Reclocked Delayed Gate or through R226 from the B Mode One-Shot. When either Pin 11 or Pin 9 of IC66 goes high, Pin 8 of IC66 goes low and causes Pin 6 of IC71 to go high, keeping Pin 8 of IC66 low. The Reset Generator remains in this state until Pin 4 of IC71 goes positive at the end of the Reset Counter cycle. Pin 6 of IC71 will move negatively causing Pin 8 of IC66 to move positively thus resetting the Reset Generator.

The set state of the Reset Generator is turned into the reset pulse by part of IC6, the Reset Buffer. Another output of the Reset Generator, Pin 13 of IC66, goes to reset the Main Gate Latch and enables the Reset Counter. The negative-going signal at Pin 8 of IC66 is inverted to a positive-going signal at Pin 3 of IC6 to provide a buffered reset to the Programmed Delay circuitry.

The positive-going signal at Pin 13 of IC66 causes Pin 6 of IC74 to go low, allowing Ø3 at Pin 6 of IC73 to clock IC73, a dual type D master-slave flip-flop. Previous to the reset pulse, S1, Pin 5 of IC73, was held high by IC74 causing Q1, Pin 3 of IC73, to be high. With the set input present, Pin 3 stays low for the duration of the set input regardless of the transitions from Ø3 at Pin 6 of IC73. At the beginning of reset, Ø3 is allowed to clock Q1 which changes state at each clock pulse. This is made possible by the connection of Pin 3 to Pin 7, the $\overline{Q}_1$ to D1 connection. $\overline{Q}_1$ is also connected to Pin 11, the clock input for the second flip-flop, Q2. This flip-flop is also connected as a D flip-flop with $\overline{Q}_2$ connected to D2, Pin 14 to Pin 10. When $\overline{Q}_1$ changes from 0 to 1, it causes Q2 to change state. These two flip-flops are connected as a series binary counter.

When $\overline{Q}_2$ moves from 0 to 1, it acts as a clock for one of the flip-flops in IC72, a dual JK AC coupled flip-flop. This clock at Pin 4 of IC72 changes the state of Pin 7 ($\overline{J}_3 = \overline{K}_3 = 0$, $C_3 = 1$) which, in turn, acts as a clock for the second flip-flop in IC72. The positive transitions into Pin 12 of IC72, C_4, causes Pin 9, the output of the fourth flip-flop, to change state. When Pins 3 and 15 of IC73 and Pins 9 and 7 of IC72 are low, Pin 8 of IC74 moves high to reset the Reset Generator. This corresponds to a count of 1101 or 13. When the Reset Generator resets, Pin 13 of IC66 moves low.

The Reset Counter stops counting when Pins 10 and 3 of IC73 move low and Pin 6 of IC74 moves high. This occurs when the Reset Counter has counted up to 1111. The counter is now locked in this position by the set input at Pin 5 of IC73 and will count to 1101 during the next reset cycle. Thus, the total count in the Reset Counter is 14 and causes a reset pulse of 140 ns. Ø3 is generated by the Gated Clock Gate and is the inverse of Ø1.

3.3.9 PROGRAMMED DELAY LINE and PROGRAMMED DELAY LINE BUFFER

(Refer to Schematic 7040-16 in Section 5.)

The signal from the Reclocked Delayed Gate becomes a differentiated spike at the bases of Q65 and Q66, the inputs to the Programmed Delay Line. The Programmed Delay Lines are arranged in a 4-2-2-1 code to allow the use of short delay lines. Throughout the Programmed Delay Line, the signal is either routed through the delay lines or around them. The front panel

DELAY controls or the remote inputs determine which of these delay lines are shunted. The front panel switches and the remote inputs are decoded from their 8-4-2-1 format by IC77.

IC76 is a quad latch that stores the delay information and enables or disables the emitter followers in the delay line circuitry. For example, if the emitter supply of Q66 is held near ground and the emitter supply of Q65 is at a high level, the positive pulse at the common base of Q65, Q66 will be passed only by Q66 to the common base of Q67, Q68. On the other hand, if the emitter supply of Q65 was near ground and the supply of Q66 was at a high level, the positive pulse at the common base of Q65, Q66 will be conducted only by Q65 and transmitted down the 1 ns Delay Line to appear at the common base of Q66, Q67 1 ns later.

During reset, the negative signal at the emitter of Q87 causes Q87 to turn on and Q88 to turn off. This positive waveform at Pins 4 and 13 of IC76 is a data strobe that allows the outputs of the quad latch to be controlled by the inputs on the data lines. When the reset pulse disappears, the outputs of the quad latch remain at the states determined by the data inputs.

Figure 3-2 can be used as a guide in determining how IC77 changes the BCD format to a 4-2-2-1 code. Notice that Q1 equals Q_1' for all decimal numbers and, as a result, this least significant bit passes undecoded to Pin 2 of IC76.

The line from Pin 12 of IC10 determines whether the front panel or remote inputs set the quad latch. When this input is high, all the outputs from each of the IC78 DTL gates are low with an open circuit or a high level present at Pins 1, 2, 19 and 20 of J1. When a low level or short circuit is present at Pins 1, 2, 19 or 20, the respective outputs of the IC78 gates will

FIG. 3-2

DEC. NO.	Q_4 8	Q_3 4	Q_2 2	Q_1 1	Q_4' 4	Q_3' 2	Q_2' 2	Q_1' 1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	1	0	0	0
5	0	1	0	1	1	0	0	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1

be high. With the signal from Pin 12 of IC10 high, D99 - D102 are back biased making the front panel controls ineffective.

When a low voltage from Pin 12 of IC10 is present, the quad latches can be turned on through diodes D99 - D102. At the same time, the outputs from the IC78 gates are not controlled by the remote inputs.

For example, when Pin 1 of J1 is high and Pin 12 of IC10 is high, Pin 6 of IC78 is low causing Pin 16 of IC76 to be low and Pin 1 of IC76 to be high. Thus, the signal is delayed by DL4. If Pin 12 of IC10 is again high but Pin 1 of J1 is low, Pin 6 of IC78 will be high causing Pin 1 of IC76 to be low and Pin 16 of IC76 to be high. This results in no delay. When Pin 12 of IC10 is low and Pin 2 of IC76 is connected to the anode of D99 via the front panel DELAY switch, Pin 1 of IC76 is high and Pin 16 of IC76 is low.

The other bits in the units decade operate in a similar fashion but are used in decoding by IC77 before entering IC76. We have noted that the least significant bit of this units decade need not be decoded. By looking at Figure 3-2, one may note that $Q_2' = Q2 + Q4$. The OR'ing is done at Pin 3 of IC77 and the result inverted at Pin 6 of IC77. Also note that $Q_3' = Q4$ and this direct connection is made. $Q_4' = Q3 + Q4$ and this OR'ing is done at Pin 11 of IC77 and inverted at Pin 8 of IC77.

The positive spike emerges from the Programmed Delay Line at the anodes of D91 and D92. It is capacitively coupled to the base of Q73, part of an emitter coupled current pair. R241, at the base of Q74, is used as a threshold adjust to help calibrate the Programmed Delay Line. The positive spike at the base of Q73 turns off Q73 causing Q75 to turn off. The positive-going signal at the collector of Q75 sets the Delayed Pulse Width Latch. The purpose of Q86, which is saturated during the reset pulse from Q88, is to prevent switching transients that occur in the Programmed Delay Line from setting the Delayed Pulse Width Latch.

3.3.10 DELAYED PULSE CIRCUITRY

(Refer to Schematic 7040-16 in Section 5.)

The Delayed Pulse Circuitry is identical to the Initial Pulse Circuitry. Refer to Paragraph 3.3.6.

3.3.11 GATE AND GATED CLOCK CIRCUITRY

(Refer to Schematic 7040-15 in Section 5.)

The positive spike through C51 from Pin 1 of IC67 causes Pin 8 of IC61, part of the Gate Width Latch, to go negative. This, in turn, causes Pin 8 of IC62, the other gate in this RS flip-flop, to go positive holding Pin 8 of IC61 low. The input to Pins 10 and 5 of IC61 remains low until the Delayed Pulse Width Latch is set. This results in two low inputs at Pins 2 and 5 of IC62. The resulting high level at Pin 6 of IC62 moves low when the Delayed Pulse Width Latch causes Pin 1 of IC61 to move high. The positive moving waveform at Pin 10 of IC61 causes Pin 8 of IC61 to move low and hence Pin 8 of IC62 to move high, resetting the Gate Width Latch. The signal at the base of Q42 is positive between the start of the Initial Pulse Width Latch and the start of the Delayed Pulse Width Latch. Q42 and Q43 are connected as an emitter-coupled current mode pair which results in Q43 being off for the duration of the Gate period. The base of emitter follower Q44 moves high causing its outputs at the GATE connector to be high. When the signal from Pin 6 of IC62 is low, Q43 is on causing the emitter of Q44 to be at a low level. L17 is a peaking inductor used to decrease the transition times of the Gate output.

The Gated Clock Latch, IC63, was set by the Reclocked Initial Gate and is reset by the Reclocked Delayed Gate. IC63 is connected as an RS flip-flop and is also reset by the reset signal. This inhibits the Gated Clock output during update. Pin 13 of IC63 moves low when the Gated Clock Latch is set. This allows the input at Pin 5 of IC60, the Gated Clock Gate, to control the output at Pin 1 of IC60. When Pin 3 of IC60 is high, Pin 1 of IC60 is always high. With Pin 3 of IC60 low, Pin 1 of IC60 is high whenever Pin 5 of IC60 is high. The other gate in IC60 inverts Ø1 to drive the Reset Counter and Pin 5 of IC60. When the base of emitter follower Q36 moves low, the emitter moves low causing Q37 to turn off. This positive-going signal is connected to the input of Darlington Q40, Q41 and is presented to the GATED CLOCK connector. R169 and R171 help to determine the positive level of the Gated Clock output. Q39 and Q38 act as a base line

restorer. When the base line moves too positive, it tends to turn off Q39 which makes Q38 conduct less of R170 current. This results in Q37 conducting more current which causes the collector of Q37 to move lower causing the base line to move lower and be restored.

3.3.12 POWER SUPPLY

(Refer to Schematic 7040-17 in Section 5.)

The +6 and -5.2 V supplies are controlled by regulators from a capacitively filtered, full-wave rectified signal. The +6 and -5.2 regulators operate in identical fashions so only the +6 V supply will be discussed here. The supply level is determined by Zener diode D125 connected to the emitter of Q94. The emitter of Q94 holds the anode of D125 close to a diode drop below ground. The grounded base connection of Q94 offers a large current gain to Q97 which controls the series pass element, Q96. For example, when the supply moves positively, Q94 tends to turn off causing Q97 and, hence, Q96 to conduct less, reducing the supply voltage. Q98 is normally saturated but will cut off when the +6 V supply is shorted to ground. This removes current to Q97 and the 6 V supply.

Q99 and Q100 form a regulator for the +5 V supply. The supply level is determined by Zener diode D126 and series diode D127. The emitter of Q99 is approximately a diode drop below ground thus establishing the level of the 5 V supply. If the 5 V supply were to move positive, this positive moving waveform would be transmitted to the emitter of Q99 to turn Q99 off and decrease the base current in Q100.

Since the power supply levels are established by Zener diodes, the values given on the schematic are nominal values.

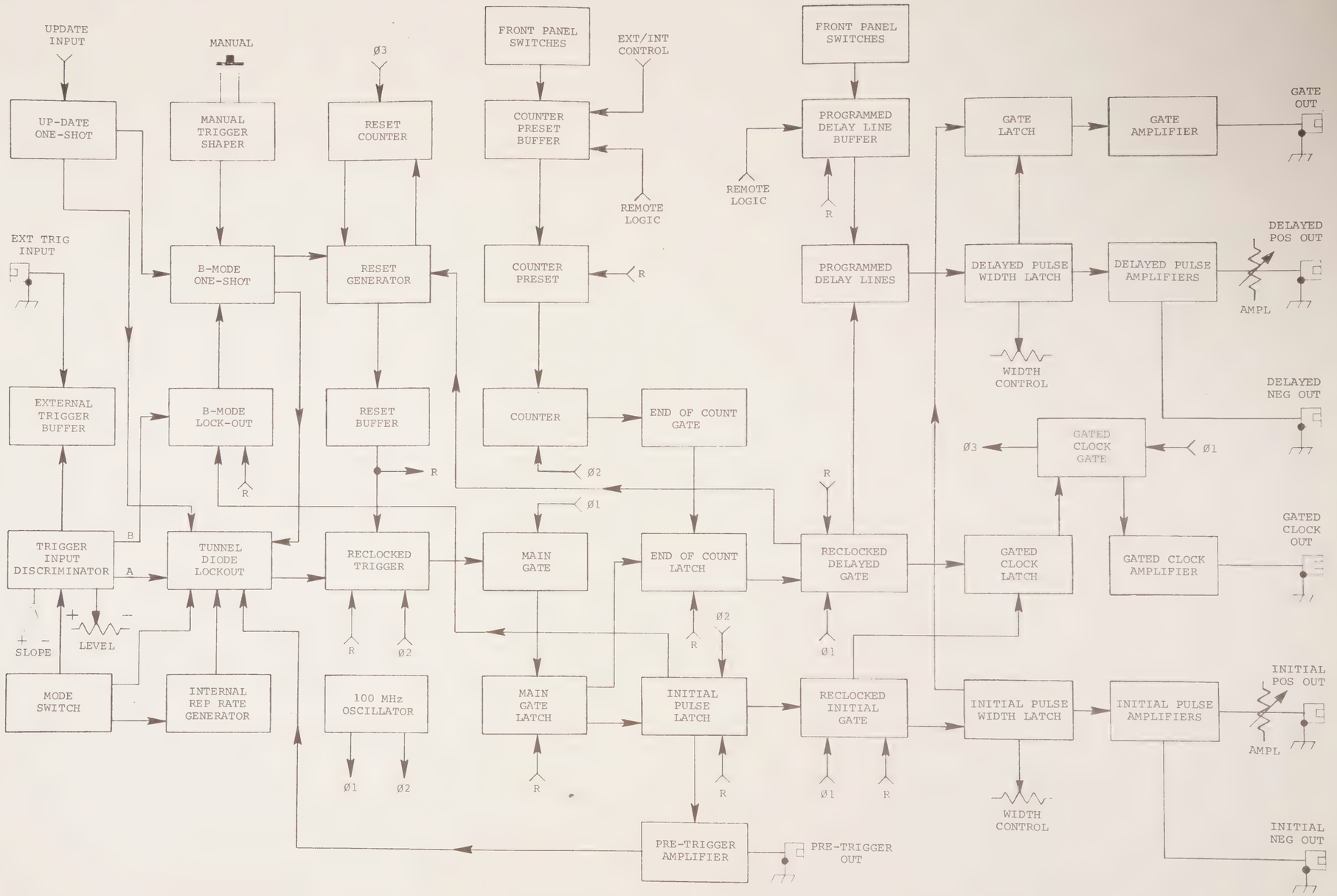


Fig., 3 – 3. Model 7040 Block Diagram

SECTION 4

MAINTENANCE

4.1 CALIBRATION

4.1.1 EQUIPMENT REQUIRED

Scope (Real Time):	Tektronix Model 454.
(Sampling):	Tektronix Model 561 with Model 3S1 Sampling Unit and Model 3T77 Sweep Unit
Probe:	Tektronix Type P6010 X10
Frequency Standard:	Frequency of 1 MHz, 10 MHz or 100 MHz. Accuracy of 1 part in 10^8 or better.
Signal Source:	Pulse or signal generator with 50 Ω output impedance and an output level adjustable from 0.2 V to 1 V peak-to-peak.
Oven:	Size to accommodate the Model 7040. Temperature Range to + 55° C. Stability ± 5° C.
Miscellaneous:	Two equal lengths (±1/2 " of RG 58A/U from 2 feet to 10 feet in length terminated in coaxial connectors.
	"T" connector, two coaxial X5 or X10, 50 Ω attenuators.

---------- NOTE ----------

The above list of equipment is intended as a guide and equipment of equivalent performance may be substituted. Not all of the above equipment is required for each calibration step. The equipment for each step is listed under its respective heading.

4.1.2 ADJUSTMENTS

The adjustment trimmers are set and sealed with glyptol prior to shipment to maintain long term calibration accuracy. It is recommended that the trimmers be resealed with the same material if this seal is broken for any reason.

The circuits and their adjustments are as follows:

100 MHz Oscillator	C8, C9
EXTERNAL TRIGGER sensitivity	R53
Internal Rate Multivibrator	R90
TD2 (D12, Tunnel Diode Bias)	R101
TD3 (D14, Tunnel Diode Bias)	R78
POS INITIAL PULSE Alignment	C50
NEG INITIAL PULSE Alignment	R213
NEG DELAYED PULSE Alignment	R275
1 ns Delays	R241 & L20 thru L23

These adjustments can easily be located by use of Figure 4-1 on the next page.

---------- NOTE ----------

Prior to calibration, all test equipment and the Model 7040 must have power applied for one hour to stabilize their parameters.

4.1.3 100 MHz OSCILLATOR

Equipment: Scope (Real Time)
Frequency Standard

Scope Setup

Vertical Sensitivity	2 V/cm
Time / Div.	0.1 μs/cm
Trigger Source	Positive, External

Model 7040 Setup

TRIGGER MODE	PERIOD
DELAY	Zero
AMPLITUDE	Maximum
WIDTH	Minimum

Connect

- Scope vertical input to Model 7040 INITIAL PULSE POS
- Scope EXT TRIGGER to frequency standard

Adjust C9 until the scope presentation does not drift to the right or left.

With the cover removed from the Model 7040, air currents will alter the 100 MHz oscillator frequency slightly; therefore, the scope presentation may move slowly to the left or right. Recheck with cover replaced.

If the C9 adjustment will not bring the 100 MHz oscillator into calibration, readjust C9 to the center of its range and adjust C8 (coarse adjust) to within C9's range, then readjust C9 as above.

----------NOTE----------

When C8 is adjusted through its entire range, it is normal for the 100 MHz oscillator to stop operating at one extreme. If for any reason C10 is replaced, it should be noted that it is a type N750 (Negative Temperature Coefficient).

4.1.4 EXTERNAL TRIGGER SENSITIVITY

Equipment:	Scope (Real Time)
	Signal Source

Scope Setup

Vertical Sensitivity	2 V / cm
Time / Div.	1 μs / cm
Trigger Source	Positive, External

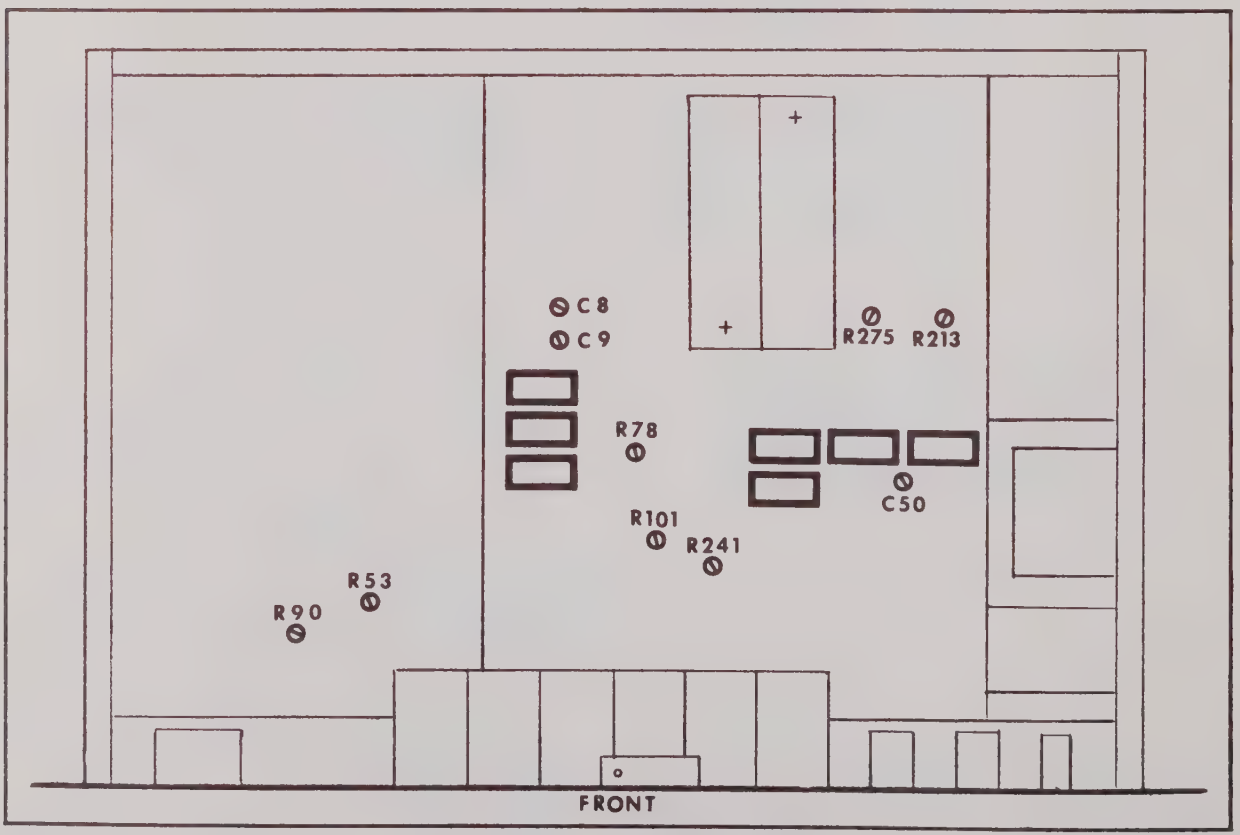


FIG. 4-1. Adjustment Location.

Signal Source Setup

Frequency	1 MHz
Amplitude	200 mV peak-to-peak

Model 7040 Setup

TRIGGER MODE	EXT TRIG A or B
DELAY	Zero
AMPLITUDE	Maximum
WIDTH	About 0.5 μs
SLOPE	Positive or Negative (determined by signal source)
TRIGGER LEVEL	Centered

Connect

- Scope vertical input to Model 7040 INITIAL PULSE POS
- Scope EXT TRIGGER inputs to 7040 PRE-TRIGGER.
- Signal source output to 7040 EXT TRIG

Adjust R53 and EXT TRIG LEVEL control so that the 7040 triggers reliably. Now remove the Signal Source from the 7040 EXT TRIG. The 7040 should NOT continue to produce an output pulse. If the 7040 continues to recycle, then R53 has not been adjusted correctly and the above procedure must be repeated.

---------- NOTE ----------

The trigger level should not be adjusted to a sensitivity less than 200 mV peak-to-peak. This will cause false triggering from system noise.

4.1.5 INTERNAL RATE MULTIVIBRATOR

Equipment: Scope (Real Time)

Scope Setup

Vertical Input	Channel 1, 2 V/cm
Time/Div.	0.1 μs/cm
Trigger Source	Positive, External

Model 7040 Setup

TRIGGER MODE	INT 5 MHz; FINE, MAX
DELAY	Zero
AMPLITUDE	Maximum
WIDTH	Minimum

Connect

- Scope vertical input to Model 7040 INITIAL PULSE POS
- External Trigger to 7040 PRE-TRIGGER

Adjust R90 so that the interval between pulses is 0.2 μs. Check the other three ranges (0.5 MHz, 50 kHz and 5 kHz) to insure that the maximum repetition rate on any range is greater than the minimum rate on the next higher range. A small readjustment of R90 may be required to obtain proper range overlap.

R90 has more effect at the high end of each range. Adjustments of R90 should be made with the FINE control at MAX.

4.1.6 TUNNEL DIODE BIAS TD2 (D12)

Equipment: Scope (Real Time)
Probe
Signal Source
Oven

Scope Setup

Vertical	Channel 1, 20 mV/cm
Time/Div.	0.1 μs/cm
Trigger Source	Positive, Internal

Model 7040 Setup

TRIGGER MODE	EXT TRIG B
DELAY	Zero
EXT TRIG LEVEL	Centered
SLOPE	Positive or Negative (Dependent on signal source)

Signal Source Setup

Frequency	1 MHz
Amplitude	1 V peak-to-peak

Oven Setup

Temperature	+55°C (+131°F)

Install 7040 in oven and allow sufficient time for temperature to stabilize.

Connect

- Scope probe to anode of TD2 (cathode is grounded)
- Signal Source to 7040 EXT TRIG

---------- NOTE ----------

Use ground lead as short as practical on probe to avoid spurious signals.

Adjust R101 for a jitter-free signal of 400 mV in amplitude and 0.1 μs in width.

4.1.7 TUNNEL DIODE BIAS TD3 (D14)

Equipment: Scope (Real Time)
Probe
Signal Source
Oven

Scope Setup

Vertical	Channel 1, 20 mV / cm
Time / Div.	0.1 μs / cm
Trigger Source	Positive, External

Model 7040 Setup

TRIGGER MODE	EXT TRIG B
DELAY	Zero
EXT TRIG LEVEL	Centered
SLOPE	Positive or Negative (Dependent on signal source)

Signal Source Setup

Frequency	1 MHz
Amplitude	1 V peak-to-peak

Oven Setup

Temperature	+55^{o}C (+131^{o}F)

Install 7040 in oven and allow sufficient time for temperature to stabilize.

Connect

- Scope EXT TRIG to 7040 PRE-TRIGGER
- Probe to Anode of TD3 (the cathode is grounded)
- Signal Source to 7040 EXT TRIG

---------- NOTE ----------

Use ground lead as short as practical on probe to avoid spurious signals.

Adjust R78 for a jitter-free signal of 400 mV in amplitude and 0.05 μs in width. Remove signal source from EXT TRIG. If the signal continues to appear at TD3, adjust R78 clockwise until the signal stops and recheck as above.

4.1.8 INITIAL AND DELAYED PULSE ALIGNMENT

Equipment: Scope (Sampling)
Two matched coax lines
Two coaxial attenuators
"T" connector

---------- **CAUTION** ----------

The positive pulse output of the 7040 may be of sufficient amplitude to damage the input of a sampling scope if attenuators are not used.

Scope Setup

Vertical Sensitivity	Dual Trace 100 mV / cm (X10 Att.) 200 mV / cm (X5 Att.)
Time / Div.	1 ns / cm
Trigger Source	Positive, External

Model 7040 Setup

TRIGGER MODE	PERIOD
DELAY	Zero
AMPLITUDE	Maximum
WIDTH	20 to 30 ns

Scope Calibration Check

Connect

- Coaxial attenuators to A and B inputs
- Matched coaxial lines to attenuators
- Both free ends of coaxial lines to "T" connector
- "T" connector to 7040 INITIAL PULSE POS
- Scope Ext Trigger to 7040 PRE-TRIGGER

Adjust the A and B channel base lines to be identical. Adjust the two channel GAINS to be identical. Now the leading edge of each trace should match exactly. If they do not:

a) Some sampling units have a B Delay adjustment. Make this adjustment until the two traces are superimposed.

b) Trim the length of one of the coax lines until the traces match exactly. Mark the cables according to the channel to which it was trimmed (A or B) so that the propagation time calibration will be maintained.

c) Refer to the scope instruction manual calibration section on Co-Channel Time Coincidence and adjust if necessary.

4.1.9 POSITIVE INITIAL PULSE ALIGNMENT

Equipment setup and connections are the same as for scope calibration except as follows:

- Set aside "T" connector
- Connect coaxial lines to 7040 INITIAL PULSE POS and DELAYED PULSE POS

Adjust C50 so that the pulses align at the 50% points.

4.1.10 INITIAL NEGATIVE PULSE ALIGNMENT

Equipment setup and connections are the same as above except as follows:

- Connect one coax line to the 7040 INITIAL PULSE POS and the other to INITIAL PULSE NEG
- Center both pulses on scope screen

Adjust R213 so that the two pulses cross at the 50% points.

4.1.11 DELAYED NEGATIVE PULSE ALIGNMENT

Equipment setup and connections are the same as above except as follows:

- Connect one coaxial line to the 7040 INITIAL PULSE NEG and the other to DELAYED PULSE NEG

Adjust R275 so that the 50% points of pulses coincide.

IMPORTANT: The alignment procedure MUST be performed in the order given as C50 affects the timing of both the Positive and Negative Initial Pulses.

4.1.12 1 ns DELAYS

If any of these adjustments are made, Pulse Alignment calibration MUST be performed.

Equipment:	Scope (Sampling)
	One X5 or X10 coaxial attenuator

Scope Setup

Vertical	Channel A, 100 mV/cm (X10 Att.)
	200 mV/cm (X5 Att.)
Time/Div.	1 ns/cm
Trigger Source	Positive, External

Model 7040 Setup

TRIGGER MODE	PERIOD
DELAY	Zero
AMPLITUDE	Maximum
WIDTH	20 to 30 ns

Allow sufficient time for scope to arrive at its operating temperature to minimize drift. Recheck the scope calibration occasionally during the 1 ns adjustments.

Scope Calibration

Connect

- Scope Ext Trigger to 7040 PRE-TRIGGER
- Scope Channel A to 7040 DELAYED PULSE POS

Center the pulse vertically and adjust the 50% point of the leading edge to cross the horizontal center line at the first vertical line on the left edge of the scope graticule. Next, without changing the scope settings, move the scope Channel A input to the 7040 GATED CLOCK OUTPUT and switch in enough delay to observe the gated clock. Minor vertical and horizontal adjustments may now have to be made to center the GATED CLOCK pulses on the scope screen.

Adjust the Scope Horizontal Gain or Variable Time / Div. so that the GATED CLOCK pulses pass through the horizontal center line at the first vertical line on the left and the last vertical line on the right. The scope is now calibrated to 10 ns for the full screen width on 1 ns / cm. Return the delay to zero and the Channel A input to the DELAYED PULSE POS and proceed with the 1 ns calibration.

1 ns Calibration

There are two types of adjustments in the 1 ns circuitry, (R241 and L20 - L23). The R241 adjustment affects all the 1 ns delays and the L20 - L23 adjustments affect the individual delay lines. Normally L20 - L23 will not require adjustment; however, R241 may require occasional minor adjustments.

If the scope calibration has just been completed, all controls and interconnections are correct. Adjust the leading edge 50% point of the delayed pulse to pass through the first vertical line on the left and the horizontal center line of the scope graticule. Advance the 1 ns delay switch one step at a time. The leading edge of the delayed pulse should pass through the scope center line at each vertical line (±1/2 minor division) progressing from left to right. If calibration is off by only a small amount, a minor adjustment of R241 is all that is required. If the circuit is totally uncalibrated, adjust R241 so that the absolute time between zero and 1 ns delay is the same as that between 8 ns and 9 ns delay and proceed as above.

If parts have been replaced in the 1 ns signal path, then individual delay line recalibration may be required. The incoming 1-2-4-8 code is converted to a 1-2-4-2 code for the 1 ns delay lines only. Figure 4-2 shows which lines are active for each delay and the associated delay adjustments.

Delay ns

Delay Line ns		1	2	3	4	5	6	7	8	9
	1	X		X		X		X		X
	2		X	X			X	X	X	X
	4				X	X	X	X	X	X
	2								X	X

Delay Adjustments

L20	1 ns
L21	Second 2 ns
L22	First 2 ns
L23	4 ns

FIG. 4-2. 1 ns Calibration

To determine which delay lines require adjustment, observe delays from zero to 9 ns and, from the chart, determine which delay line is always active for the delays that deviate more than ±1/2 minor division.

EXAMPLE: 2 ns, 3 ns and 6 ns through 9 ns delays too long;

The first 2 ns line too long;

Shorten L22;

After the individual delay lines have been calibrated, a readjustment of R241 may be necessary.

4.2 TROUBLE-SHOOTING GUIDE

The following is a general guide to aid the technician in isolating an instrument malfunction. It is recommended that the section on theory of operation be read before repair is attempted.

MALFUNCTION	POSSIBLE DEFECT
1) No pulse from any output	No power from line Power Supply 100 MHz oscillator inoperative Wire on twisted pair broken Counter circuit not functioning TD2 or TD3 Any latch not operating Reset circuit not functioning
2) 100 MHz Oscillator does not operate	C8 adjusted to one end of its range IC 4 Xtal or coil (L1)
3) Operates in MODE INT but not MODE EXT A or B	Trig input discriminator (Q6 thru Q13)
4) Operates in MODE EXT A but not MODE EXT B	Q9, Q10, Q11 or Mode Switch wire Twisted pair (70) B Mode One-shot Q1, Q14
5) Operates in MODE EXT B but not MODE EXT A	Q12 or Q13 Mode Switch wire
6) Operates in MODE EXT A and B but not INT	Q19, Q20, Q21 Mode Switch wire Twisted Pair (64)
7) Operates in MODE EXT A or B + slope only or − slope only	Q7, Q8
8) Does not operate in PERIOD MODE	Q15 Wire (71) Mode Switch
9) No GATED CLOCK Output	Gated Clock Latch IC 63 Gated Clock Gate or clock drive IC 60 Gated Clock Amplifier Q36 thru Q41

(continued)

TROUBLE-SHOOTING GUIDE (continued)

10) No PRE-TRIGGER	Broken wire to front panel
11) No GATE	Delayed pulse width time longer than repetition rate interval Gate width latch IC 67 or IC 68 Gate Amplifier Q42 thru Q44
12) No INITIAL PULSE POS or NEG	DL 3 Initial pulse latch IC 67 Width circuit Q50, Q51 Pos. Amplifier Q45 thru Q49
13) No INITIAL PULSE NEG (POS PULSE OK)	Neg. Amplifier Q52, Q53, Q54 R213 not adjusted correctly
14) No INITIAL PULSE POS (NEG PULSE OK)	Amplitude Control
15) No DELAYED PULSE POS or NEG	1 ns delay circuit Q65 thru Q75 R241 set incorrectly Width latch IC 75 Pos. Amplifier Q76 thru Q80 Width circuit Q81, Q82
16) No DELAYED PULSE NEG (POS PULSE OK)	Delayed pulse Neg. Amplifier Q83, Q84, Q85 R286 not adjusted correctly
17) No DELAYED PULSE POS (NEG PULSE OK)	Amplitude Control
18) Front Panel Delay Switches have no control or Remote has no control	Remote control J1 Pin 35 IC 10, Q1, Q2

SECTION 5

PARTS LISTS & SCHEMATICS

ABBREVIATIONS

cer	ceramic	μH	microhenry
comp	composition carbon	μF	microfarad
elec	electrolytic, metal case	pF	picofarad
mic	mica	pos	positions
myl	mylar	tan	tantalum
K	kilohm	V	working volts DC
M	megohm	var	variable
m	milli	W	watts
MF	metal film	ww	wirewound

----------NOTE----------

The last number after each part description is BERKELEY NUCLEONICS part number for re-ordering.

TRIGGER & GATE RECLOCKING CIRCUITS (Dwg. No. 7040-13)

CAPACITORS

C1	220 pF	mic	500 V	5%	112-008
C2	47 pF	mic	500 V	5%	112-003
C3	100 pF	mic	500 V	5%	112-004
C4	47 pF	mic	500 V	5%	112-003
C5	150 pF	mic	500 V	5%	112-005
C6	6.8 μF	tan	35 V		122-012
C7	15 pF	cer	1 KV	5%	110-024
C8	2-20 pF	var			130-001
C9	2-20 pF	var			130-001
C10	33 pF	mic	500 V	5%	112-002
C11	100 pF	mic	500 V	5%	112-004
C12	33 pF	mic	500 V	5%	112-002
C13	0.05 μF	cer	25 V		110-019
C14	0.05 μF	cer	25 V		110-019
C15	0.05 μF	cer	25 V		110-019
C16	0.05 μF	cer	25 V		110-019
C17	0.05 μF	cer	25 V		110-019
C18	0.05 μF	cer	25 V		110-019
C19	100 pF	mic	500 V	5%	112-004
C20	100 pF	mic	500 V	5%	112-004
C21	0.05 μF	cer	25 V		110-019
C22	100 μF	elec	16 V		120-007
C23	82 pF	mic	500 V	5%	112-020
C24	0.001 μF	myl	600 V	10%	114-001
C25	0.01 μF	myl	200 V	10%	114-025
C26	0.1 μF	myl	100 V	10%	114-020
C27	0.05 μF	cer	25 V		110-019
C28	100 μF	elec	16 V		120-007
C29	270 pF	mic	500 V	5%	112-009
C30	100 pF	mic	500 V	5%	112-004

DIODES

D1-D7	1N4152	411-004
D8	1N3719	414-002
D9-D11	1N4152	411-004
D12	1N3719	414-002
D13	1N270	411-002
D14	1N3719	414-002
D15	1N4152	411-004

INTEGRATED CIRCUITS

IC1	MC1010P	440-007
IC2	MC1004P	440-006
IC3	MC851P	440-004
IC4	MC1026P	440-010
IC5	MC1023P	440-009
IC6	MC1010P	440-007

INDUCTORS

L1	Special	
L2	0.33 μH	310-011
L3	1.8 μH	310-010
L4	2.2 μH	310-005
T1	Special	

TRANSISTORS

Q4	2N4258	430-030
All other PNP are 2N3640		430-026
All other NPN are 2N3646		430-027

RESISTORS

R1	390 Ω	1/4 W	comp	5%	213-391	R51	220 Ω	1/4 W	comp	5%	213-221
R2	3.9 K	1/4 W	comp	5%	213-392	R52	220 Ω	1/4 W	comp	5%	213-221
R3	3.9 K	1/4 W	comp	5%	213-392	R53	50 Ω	1/2 W	var		244-018
R4	1.8 K	1/4 W	comp	5%	213-182	R54	15 Ω	1/4 W	comp	5%	213-150
R5	3.3 K	1/4 W	comp	5%	213-332	R55	470Ω	1/4 W	comp	5%	213-471
R6	1 K	1/4 W	comp	5%	213-102	R56	1 K	1/4 W	comp	5%	213-102
R7	3.3 K	1/4 W	comp	5%	213-332	R57	470 Ω	1/4 W	comp	5%	213-471
R8	330 Ω	1/4 W	comp	5%	213-331	R58	2.2 K	1/4 W	comp	5%	213-222
R9	1.8 K	1/4 W	comp	5%	213-182	R59	47 Ω	1/4 W	comp	5%	213-470
R10	3.3 K	1/4 W	comp	5%	213-332	R60	820 Ω	1/4 W	comp	5%	213-821
R11	470 Ω	1/4 W	comp	5%	213-471	R61	1 K	1/4 W	comp	5%	213-102
R12	390 Ω	1/4 W	comp	5%	213-391	R62	470 Ω	1/4 W	comp	5%	213-471
R13	820 Ω	1/4 W	comp	5%	213-821	R63	1 K	1/4 W	comp	5%	213-102
R14	100 Ω	1/4 W	comp	5%	213-101	R64	330 Ω	1/4 W	comp	5%	213-331
R15	560 Ω	1/4 W	comp	5%	213-561	R65	680 Ω	1/4 W	comp	5%	213-681
R16	82 Ω	1/4 W	comp	5%	213-820	R66	2.2 K	1/4 W	comp	5%	213-222
R17	680 Ω	1/4 W	comp	5%	213-681	R67	56 Ω	1/4 W	comp	5%	213-560
R18	3.3 K	1/4 W	comp	5%	213-332	R68	1 K	1/4 W	comp	5%	213-102
R19	4.7 K	1/4 W	comp	5%	213-472	R69	4.7 K	1/4 W	comp	5%	213-472
R20	3.9 K	1/4 W	comp	5%	213-392	R70	470 Ω	1/4 W	comp	5%	213-471
R21	330 Ω	1/4 W	comp	5%	213-331	R71	1 K	1/4 W	comp	5%	213-102
R22	330 Ω	1/4 W	comp	5%	213-331	R72	470 Ω	1/4 W	comp	5%	213-471
R23	330 Ω	1/4 W	comp	5%	213-331	R73	220 Ω	1/4 W	comp	5%	213-221
R24	120 Ω	1/4 W	comp	5%	213-121	R74	3.3 K	1/4 W	comp	5%	213-332
R25	82 Ω	1/4 W	comp	5%	213-820	R75	470 Ω	1/4 W	comp	5%	213-471
R26	120 Ω	1/4 W	comp	5%	213-121	R76	220 Ω	1/4 W	comp	5%	213-221
R27	270 Ω	1/4 W	comp	5%	213-271	R77	560 Ω	1/4 W	comp	5%	213-561
R28	100 Ω	1/4 W	comp	5%	213-101	R78	200 Ω	1/2 W	var		244-019
R29	3.3 K	1/4 W	comp	5%	213-332	R79	680 Ω	1/4 W	comp	5%	213-681
R30	470 Ω	1/4 W	comp	5%	213-471	R80	12 Ω	1/4 W	comp	5%	213-120
R31	390 Ω	1/4 W	comp	5%	213-391	R81	1 K	1/4 W	comp	5%	213-102
R32	100 Ω	1/4 W	comp	5%	213-101	R82	270 Ω	1/4 W	comp	5%	213-271
R33	56 Ω	1/4 W	comp	5%	213-560	R83	3.9 K	1/4 W	comp	5%	213-392
R34	470 Ω	1/4 W	comp	5%	213-471	R84	4.7 Ω	1/4 W	comp	5%	213-047
R35	33 Ω	1/4 W	comp	5%	213-330	R85	330 Ω	1/4 W	comp	5%	213-331
R36	390 Ω	1/4 W	comp	5%	213-391	R86	270 Ω	1/4 W	comp	5%	213-271
R37	3.3 K	1/4 W	comp	5%	213-332	R87	330 Ω	1/4 W	comp	5%	213-331
R38	68 Ω	1/2 W	comp	5%	212-680	R88	4.7 Ω	1/4 W	comp	5%	213-047
R39	470 Ω	1/4 W	comp	5%	213-471	R89	51 Ω	1/4 W	comp	5%	213-510
R40	470 Ω	1/4 W	comp	5%	213-471	R90	200 Ω	1/2 W	var		244-019
						R91	5 K	2 W	var		240-010
R41	47 Ω	1/4 W	comp	5%	213-470	R92	51 Ω	1/4 W	comp	5%	213-510
R42	220 Ω	1/4 W	comp	5%	213-221	R93	390 Ω	1/4 W	comp	5%	213-391
R43	100 Ω	1/4 W	comp	5%	213-101	R94	150 Ω	1/4 W	comp	5%	213-151
R44	100 Ω	1/4 W	comp	5%	213-101	R95	18 Ω	1/4 W	comp	5%	213-180
R45	360 Ω	1/4 W	comp	5%	213-361						
						R96	18 Ω	1/4 W	comp	5%	213-180
R46	560 Ω	1/4 W	comp	5%	213-561	R97	560 Ω	1/4 W	comp	5%	213-561
R47	1 K	2 W	var		240-008	R98	51 Ω	1/4 W	comp	5%	213-510
R48	390 Ω	1/4 W	comp	5%	213-391	R99	150 Ω	1/4 W	comp	5%	213-151
R49	390 Ω	1/4 W	comp	5%	213-391	R100	270 Ω	1/4 W	comp	5%	213-271
R50	220 Ω	1/4 W	comp	5%	213-221	R101	200 Ω	1/2 W	var		244-019
						R102	1K	1/4 W	comp	5%	213-102

REMOTE PROGRAM & COUNTER (Dwg. No. 7040-14)

DIODES

D20-D60	1N4152	411-004

INTEGRATED CIRCUITS

IC1	MC1010P	440-007
IC10	MC837P	440-002
IC11	MC837P	440-002
IC12	MC1812P	440-013
IC13	MC863P	440-005
IC14	MC837P	440-002
IC15	MC837P	440-002
IC16	MC863P	440-005
IC17	MC837P	440-002
IC18	MC1812P	440-013
IC19	MC837P	440-002
IC21	MC1010P	440-007
IC22	MC1010P	440-007
IC23	MC1034P	440-012
IC24	MC1013P	440-008
IC25	MC1010P	440-007
IC26	MC1013P	440-008
IC27	MC1013P	440-008
IC28	MC1010P	440-007
IC29	MC1010P	440-007
IC30	MC1013P	440-008
IC31	MC1013P	440-008
IC32	MC1010P	440-007
IC33	MC1013P	440-008
IC34	MC1013P	440-008
IC35	MC1010P	440-007
IC36	MC1010P	440-007
IC37	MC1013P	440-008
IC38	MC1013P	440-008
IC39	MC1010P	440-007
IC40	MC1013P	440-008
IC41	MC1013P	440-008
IC42	MC1010P	440-007
IC43	MC1010P	440-007
IC44	MC1013P	440-008
IC45	MC1013P	440-008
IC46	MC1010P	440-007
IC47	MC1013P	440-008
IC48	MC1013P	440-008
IC49	MC1010P	440-007
IC50	MC1010P	440-007
IC51	MC1013P	440-008
IC52	MC1013P	440-008
IC53	MC1010P	440-007
IC54	MC1013P	440-008
IC55	MC1013P	440-008
IC56	MC1023P	440-009
IC57	MC1004P	440-006
IC58	MC1004P	440-006

TRANSISTORS

Q30	2N3640	430-026
Q31	2N3640	430-026

RESISTORS

R110	180 Ω	1/4 W	comp	5%	213-181
R111	390 Ω	1/4 W	comp	5%	213-391
R112	330 Ω	1/4 W	comp	5%	213-331
R113	330 Ω	1/4 W	comp	5%	213-331
R114 - R134 are:					
	4.7 K	1/4 W	comp	5%	213-472
R135 - R154 are:					
	6.8 K	1/4 W	comp	5%	213-682

INITIAL, GATE, & GATED CLOCK (Dwg. No. 7040-15)

CAPACITORS

C40	0.05 μF	cer	25 V		110-019	C50	2-20 pF	var			130-001
C41	0.05 μF	cer	25 V		110-019	C51	47 pF	mic	500 V	5%	112-003
C42	5 μF	elec	25 V		120-004	C52	5 μF	elec	25 V		120-004
C43	5 μF	elec	25 V		120-004	C53	100 μF	elec	16 V		120-007
C44	0.05 μF	cer	25 V		110-019	C54	0.05 μF	cer	25 V		110-019
C45	0.05 μF	cer	25 V		110-019	C55	0.05 μF	cer	25 V		110-019
C46	5 μF	elec	25 V		120-004	C56	330 pF	mic	500 V	5%	112-010
C47	68 pF	mic	500 V	5%	112-018	C57	0.05 μF	cer	25 V		110-019
C48	0.05 μF	cer	25 V		110-019	C58	0.05 μF	cer	25 V		110-019
C49	0.05 μF	cer	25 V		110-019	C59	0.05 μF	cer	25 V		110-019

(Dwg. No. 7040-15 continued)

DIODES

D70	1N4152	411-004
D71	1N4152	411-004
D72	FH 1100	415-001
D73	FH 1100	415-001
D74	1N4152	411-004
D75	1N4152	411-004
D76	1N4152	411-004
D77	1N4152	411-004
D78	1N4152	411-004

DELAY LINES

DL1	15 ns	Special
DL2	5 ns	Special

INTEGRATED CIRCUITS

IC60	MC1023P	440-009
IC61	MC1023P	440-009
IC62	MC1023P	440-009
IC63	MC1023P	440-009
IC64	MC1034P	440-012
IC65	MC1023P	440-009
IC66	MC1023P	440-009
IC67	MC1023P	440-009

INDUCTORS

L15	0.33 μH
L16	0.33 μH
L17	0.47 μH
L18	1 μH
L19	0.15 μH

TRANSISTORS

Q36	2N3640	430-026
Q37	2N3646	430-027
Q38	2N3646	430-027
Q39	2N3640	430-026
Q40	2N3646	430-027
Q41	2N3646	430-027
Q42	2N3646	430-027
Q43	2N3646	430-027
Q44	2N5109	430-024
Q45	2N3640	430-026
Q46	2N3646	430-027
Q47	2N3646	430-027
Q48	2N3640	430-026
Q49	2N3646	430-027
Q50	2N3640	430-026
Q51	2N3640	430-026
Q52	2N3646	430-027
Q53	2N3646	430-027
Q54	2N3640	430-026

RESISTORS

R165	39 Ω	1/4 W	comp	5%	213-390
R166	470 Ω	1/4 W	comp	5%	213-471
R167	820 Ω	1/4 W	comp	5%	213-821
R168	150 Ω	1/4 W	comp	5%	213-151
R169	270 Ω	1/4 W	comp	5%	213-271
R170	220 Ω	1/4 W	comp	5%	213-221
R171	270 Ω	1/4 W	comp	5%	213-271
R172	560 Ω	1/4 W	comp	5%	213-561
R173	560 Ω	1/4 W	comp	5%	213-561
R174	100 Ω	1/4 W	comp	5%	213-101
R175	100 Ω	1/4 W	comp	5%	213-101
R176	150 Ω	1/4 W	comp	5%	213-151
R177	330 Ω	1/4 W	comp	5%	213-331
R178	100 Ω	1/4 W	comp	5%	213-101
R179	330 Ω	1/4 W	comp	5%	213-331
R180	4.7 Ω	1/4 W	comp	5%	213-047
R181	470 Ω	1/4 W	comp	5%	213-471
R182	39 Ω	1/4 W	comp	5%	213-390
R183	56 Ω	1/4 W	comp	5%	213-560
R184	56 Ω	1/4 W	comp	5%	213-560
R185	56 Ω	1/4 W	comp	5%	213-560
R186	300 Ω	1/4 W	comp	5%	213-301
R187	680 Ω	1/4 W	comp	5%	213-681
R188	39 Ω	1/4 W	comp	5%	213-390
R189	470 Ω	1/4 W	comp	5%	213-471
R190	150 Ω	1/4 W	comp	5%	213-151
R191	820 Ω	1/4 W	comp	5%	213-821
R192	150 Ω	1/4 W	comp	5%	213-151
R193	100 Ω	1/4 W	comp	5%	213-101
R194	560 Ω	1/4 W	comp	5%	213-561
R195	560 Ω	1/4 W	comp	5%	213-561
R196	4.7 Ω	1/4 W	comp	5%	213-047
R197	330 Ω	1/4 W	comp	5%	213-331
R198	330 Ω	1/4 W	comp	5%	213-331
R199	51 Ω	1 W	comp	5%	211-510
R200	51 Ω	1/2 W	comp	5%	212-510
R201A & R201B	50 Ω		var		240-009
R202	2.2 K	1/4 W	comp	5%	213-222
R203	1 K	1/4 W	comp	5%	213-102
R204	470 Ω	1/4 W	comp	5%	213-471
R205	1 K	2 W	var		240-008
R206	390 Ω	1/4 W	comp	5%	213-391
R207	180 Ω	1/4 W	comp	5%	213-181
R208	1.2 K	1/4 W	comp	5%	213-122
R209	180 Ω	1/4 W	comp	5%	213-181
R210	150 Ω	1/4 W	comp	5%	213-151
R211	82 Ω	1/4 W	comp	5%	213-820
R212	150 Ω	1/4 W	comp	5%	213-151
R213	200 Ω	1/2 W	var		244-019
R214	150 Ω	1/4 W	comp	5%	213-151
R215	56 Ω	1/4 W	comp	5%	213-560
R216	22 Ω	1/4 W	comp	5%	213-220

DELAYED PULSE & RESET (Dwg. No. 7040-16)

CAPACITORS

C65	270 pF	mic	500 V	5%	112-009
C66	47 pF	mic	500 V	5%	112-003
C67	0.05 μF	cer	25 V		110-019
C68	470 pF	cer	1 KV	10%	110-010
C69	270 pF	mic	500 V	5%	112-009
C70	270 pF	mic	500 V	5%	112-009
C71	5 μF	elec	25 V		120-004
C72	100 μF	elec	16 V		120-007
C73	0.05 μF	cer	25 V		110-019
C74	0.05 μF	cer	25 V		110-019
C75	0.05 μF	cer	25 V		110-019
C76	330 pF	mic	500 V	5%	112-010
C77	0.05 μF	cer	25 V		110-019
C78	100 pF	mic	500 V	5%	112-004

DIODES

D85-D92	1N4152	411-004
D93	1N270	411-002
D94	1N4152	411-004
D95	FH 1100	415-001
D96	1N4152	411-004
D97	1N4152	411-004
D98	1N4152	411-004
D99	1N270	411-002
D100	1N270	411-002
D101	1N270	411-002
D102	1N270	411-002
D103	1N4152	411-004

DELAY LINES

DL4	1 ns	Special
DL5	2 ns	Special
DL6	2 ns	Special
DL7	4 ns	Special
DL8	7 ns	Special

INTEGRATED CIRCUITS

IC6	MC1010P	440-007
IC66	MC1023P	440-009
IC70	MC1027P	440-011
IC71	MC1023P	440-009
IC72	MC1032P	440-014
IC73	MC10131L	440-015
IC74	MC1023P	440-009
IC75	MC1023P	440-009
IC76	MC7475P	440-016
IC77	MC846P	440-003
IC78	MC846P	440-003

INDUCTORS

L20		Special
L21		Special
L22		Special
L23		Special
L24	0.33 μH	310-011
L25	0.33 μH	310-011
L26	1 μH	310-003
L27	0.15 μH	310-001

TRANSISTORS

Q77	2N3646	430-027
Q80	2N5109	430-024
Q85	2N4258	430-030
All other PNP are:	2N3640	430-026
All other NPN are:	2N3646	430-027

RESISTORS

R225	56 Ω	1/4 W	comp	5%	213-560
R226	27 Ω	1/4 W	comp	5%	213-270
R227	1.2 K	1/4 W	comp	5%	213-122
R228	1.2 K	1/4 W	comp	5%	213-122
R229	1.2 K	1/4 W	comp	5%	213-122
R230	470 Ω	1/4 W	comp	5%	213-471
R231	39 Ω	1/4 W	comp	5%	213-390
R232	470 Ω	1/4 W	comp	5%	213-471
R233	820 Ω	1/4 W	comp	5%	213-821
R234	150 Ω	1/4 W	comp	5%	213-151
R235	100 Ω	1/4 W	comp	5%	213-101
R236	150 Ω	1/4 W	comp	5%	213-151
R237	560 Ω	1/4 W	comp	5%	213-561
R238	560 Ω	1/4 W	comp	5%	213-561
R239	4.7 Ω	1/4 W	comp	5%	213-047
R240	330 Ω	1/4 W	comp	5%	213-331
R241	50 Ω	1/2 W	var		244-018
R242	51 Ω	1 W	comp	5%	211-510
R243A & R243B	50 Ω		var		240-009
R244	51 Ω	1/2 W	comp	5%	212-510
R245	1 K	1/4 W	comp	5%	213-102
R246	470 Ω	1/4 W	comp	5%	213-471
R247	1 K	2 W	var		240-008
R248	390 Ω	1/4 W	comp	5%	213-391
R249	560 Ω	1/4 W	comp	5%	213-561
R250	100 Ω	1/4 W	comp	5%	213-101
R251	560 Ω	1/4 W	comp	5%	213-561
R252	4.7 K	1/4 W	comp	5%	213-472
R253	560 Ω	1/4 W	comp	5%	213-561
R254	82 Ω	1/4 W	comp	5%	213-820

(Continued)

(Dwg. No. 7040-16 continued)

R255	2.2 K	1/4 W	comp	5%	213-222
R256	390 Ω	1/4 W	comp	5%	213-391
R257	390 Ω	1/4 W	comp	5%	213-391
R258	560 Ω	1/4 W	comp	5%	213-561
R259	100 Ω	1/4 W	comp	5%	213-101
R260	390 Ω	1/4 W	comp	5%	213-391
R261	390 Ω	1/4 W	comp	5%	213-391
R262	560 Ω	1/4 W	comp	5%	213-561
R263	100 Ω	1/4 W	comp	5%	213-101
R264	390 Ω	1/4 W	comp	5%	213-391
R265	390 Ω	1/4 W	comp	5%	213-391
R266	560 Ω	1/4 W	comp	5%	213-561
R267	100 Ω	1/4 W	comp	5%	213-101
R268	390 Ω	1/4 W	comp	5%	213-391
R269	390 Ω	1/4 W	comp	5%	213-391
R270	4.7 Ω	1/4 W	comp	5%	213-047
R271	560 Ω	1/4 W	comp	5%	213-561
R272	180 Ω	1/4 W	comp	5%	213-181
R273	470 Ω	1/4 W	comp	5%	213-471
R274	560 Ω	1/4 W	comp	5%	213-561
R275	200 Ω	1/2 W	var		244-019
R276	330 Ω	1/4 W	comp	5%	213-331
R277	1 K	1/4 W	comp	5%	213-102
R278	470 Ω	1/4 W	comp	5%	213-471
R279	47 Ω	1/4 W	comp	5%	213-470
R280	1 K	1/4 W	comp	5%	213-102
R281	470 Ω	1/4 W	comp	5%	213-471
R282	390 Ω	1/4 W	comp	5%	213-391
R283	180 Ω	1/4 W	comp	5%	213-181
R284	180 Ω	1/4 W	comp	5%	213-181
R285	150 Ω	1/4 W	comp	5%	213-151
R286	1 K	1/4 W	comp	5%	213-103
R287	1.2 K	1/4 W	comp	5%	213-122
R288	150 Ω	1/4 W	comp	5%	213-151
R289	82 Ω	1/4 W	comp	5%	213-820
R291	150 Ω	1/4 W	comp	5%	213-151
R292	2.2 K	1/4 W	comp	5%	213-222

POWER SUPPLY (Dwg. No. 7040-17)

CAPACITORS

C80	8000 μF	elec	15 V	120-009
C81	8000 μF	elec	15 V	120-009
C82	0.001 μF	cer	1 KV	110-011
C83	0.001 μF	cer	1 KV	110-011
C84	100 μF	elec	16 V	120-007
C85	0.005 μF	cer	1 KV	110-013
C86	100 μF	elec	16 V	120-007

DIODES

D120-D123	PA 10	10 AMP RECT	410-005
D124	1N5234		412-010
D125	1N4736		413-002
D126	1N5231		412-009
D127	1N4152		411-004

INDUCTORS

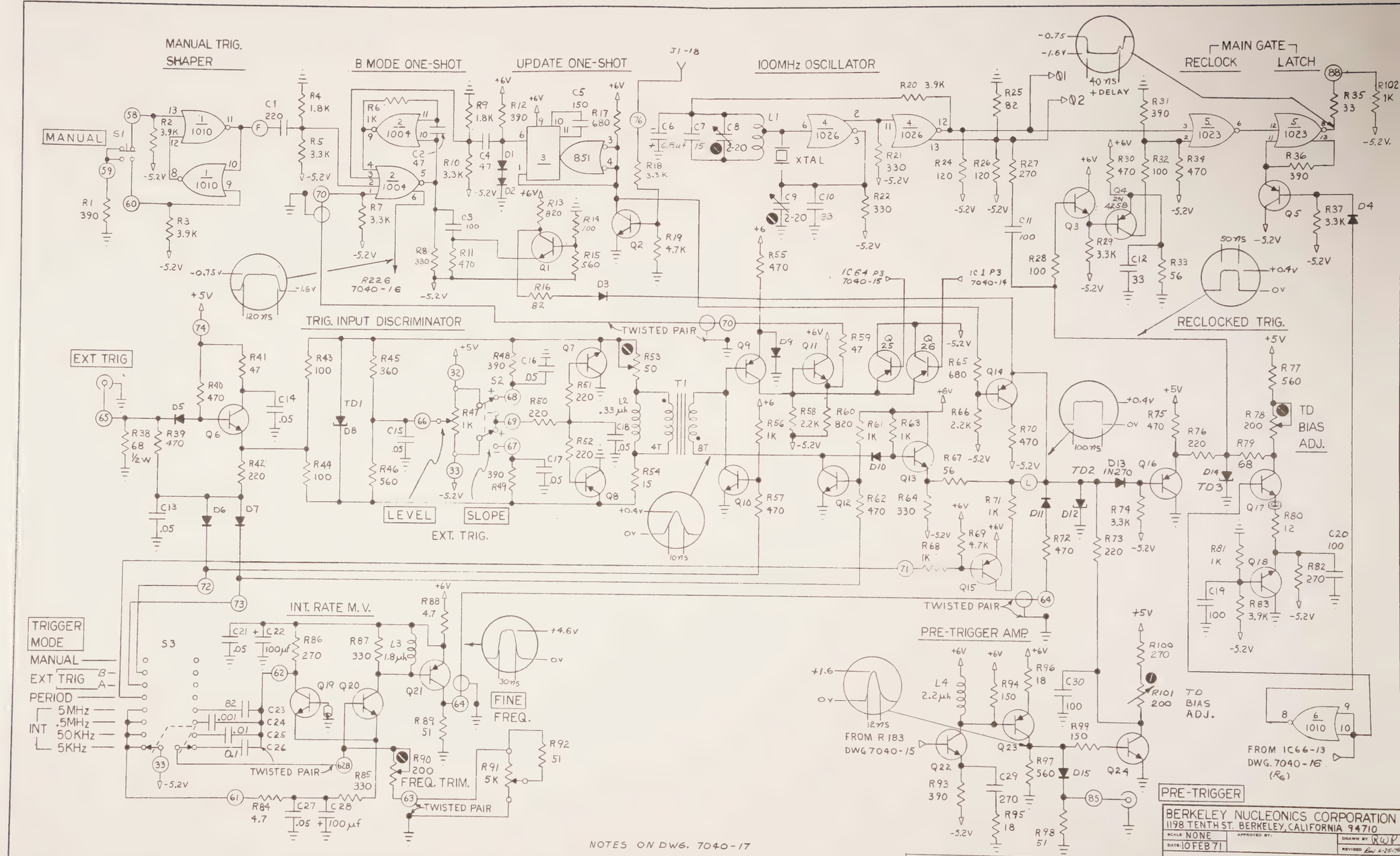
T2	Power Transformer	320-004

TRANSISTORS

Q90	2N2219	430-006
Q91	TIP33A	430-028
Q92	2N3640	430-026
Q93	2N3640	430-026
Q94	2N3646	430-027
Q96	TIP34A	430-029
Q97	2N2905	430-008
Q98	2N3646	430-027
Q99	2N3646	430-027
Q100	2N2905	430-008

RESISTORS

R300	100 Ω	1/4 W	comp	5%	213-101
R301	39 Ω	2 W	comp	5%	210-390
R302	680 Ω	1/4 W	comp	5%	213-681
R303	560 Ω	1/4 W	comp	5%	213-561
R304	680 Ω	1/4 W	comp	5%	213-681
R305	100 Ω	1 W	comp	5%	211-101
R306	2.2 K	1/4 W	comp	5%	213-222
R307	1 K	1/4 W	comp	5%	213-102
R308	1 K	1/4 W	comp	5%	213-102
R309	470 Ω	1/4 W	comp	5%	213-471



NO.	DATE	DESCRIPTION	BY
A	6-25-75	MISC. CORR.	RWJ

REVISIONS

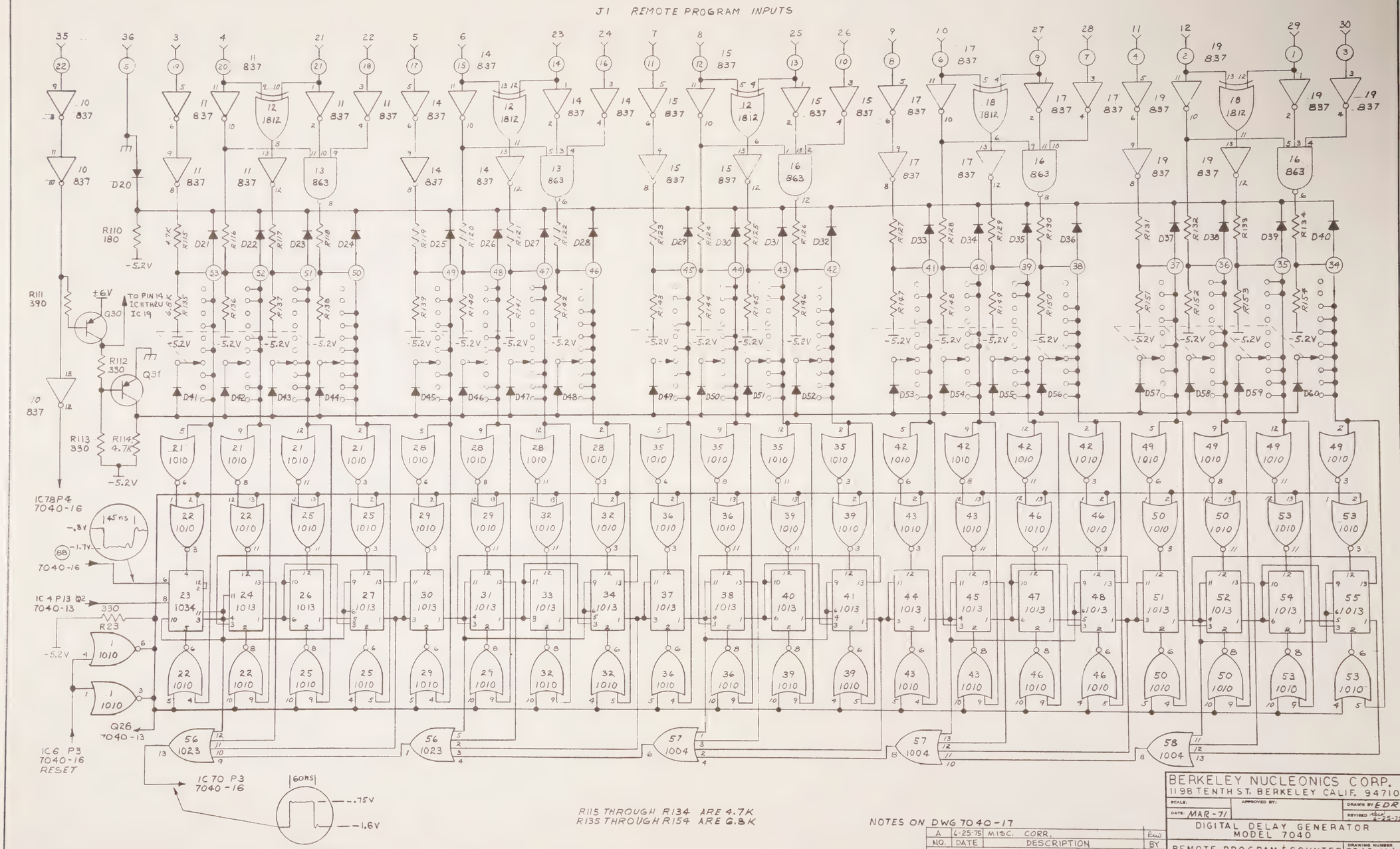
BERKELEY NUCLEONICS CORPORATION
1198 TENTH ST. BERKELEY, CALIFORNIA 94710

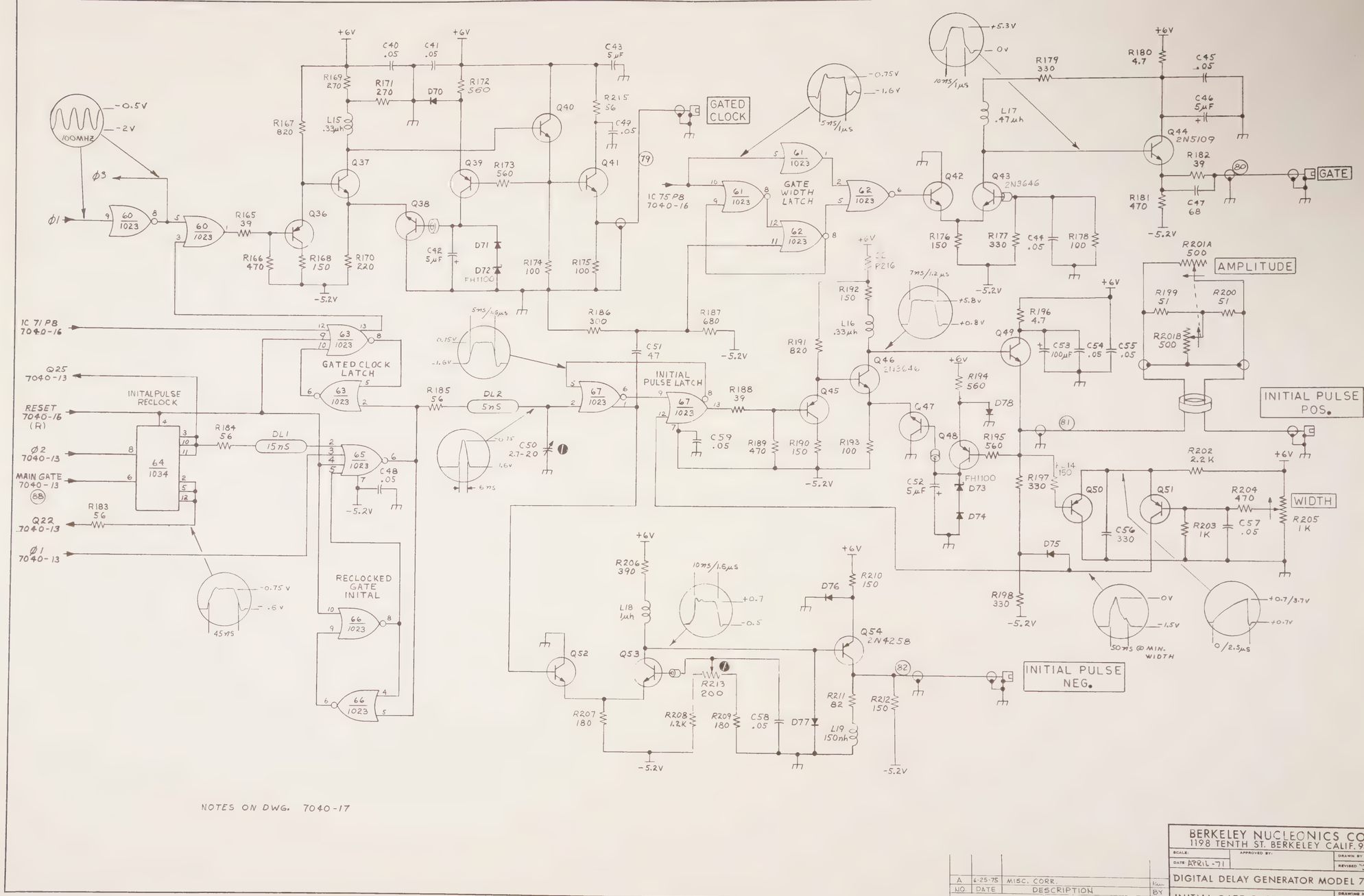
SCALE NONE | APPROVED BY: | DRAWN BY RWJ
DATE 10 FEB 71 | REVISED (Ltr) 6-25-75

DIGITAL DELAY GENERATOR MODEL 7040

TRIG. & GATE RECLOCKING CIRCUITS | DRAWING NUMBER 7040-13A

LUCAS PRINTED ON NO. 1000H CLEARPRINT


J1 REMOTE PROGRAM INPUTS
R110 180
R111 390
R112 330
R113 330
R114 4.7K
R115 4.7K
R116 6.8K
R135 6.8K
R23 330
+6V
-5.2V
Q30
Q31
Q26
D20
TO PIN 14 OF IC 11 THRU IC 19
IC 7 8 P 4 7040-16
IC 4 P 13 7040-13
IC 6 P 3 7040-16 RESET
IC 7 0 P 3 7040-16
45ns
60ns
-.8V
-1.7V
-.75V
-1.6V
R115 THROUGH R134 ARE 4.7K
R135 THROUGH R154 ARE 6.8K
NOTES ON DWG 7040-17
A 6-25-75 MISC. CORR. RW
NO. DATE DESCRIPTION BY
REVISIONS
BERKELEY NUCLEONICS CORP.
1198 TENTH ST. BERKELEY CALIF. 94710
SCALE:
APPROVED BY:
DRAWN BY EDR
DATE: MAR-71
REVISED 6-25-75
DIGITAL DELAY GENERATOR
MODEL 7040
REMOTE PROGRAM & COUNTER
DRAWING NUMBER 7040-14A



NOTES ON DWG. 7040-17

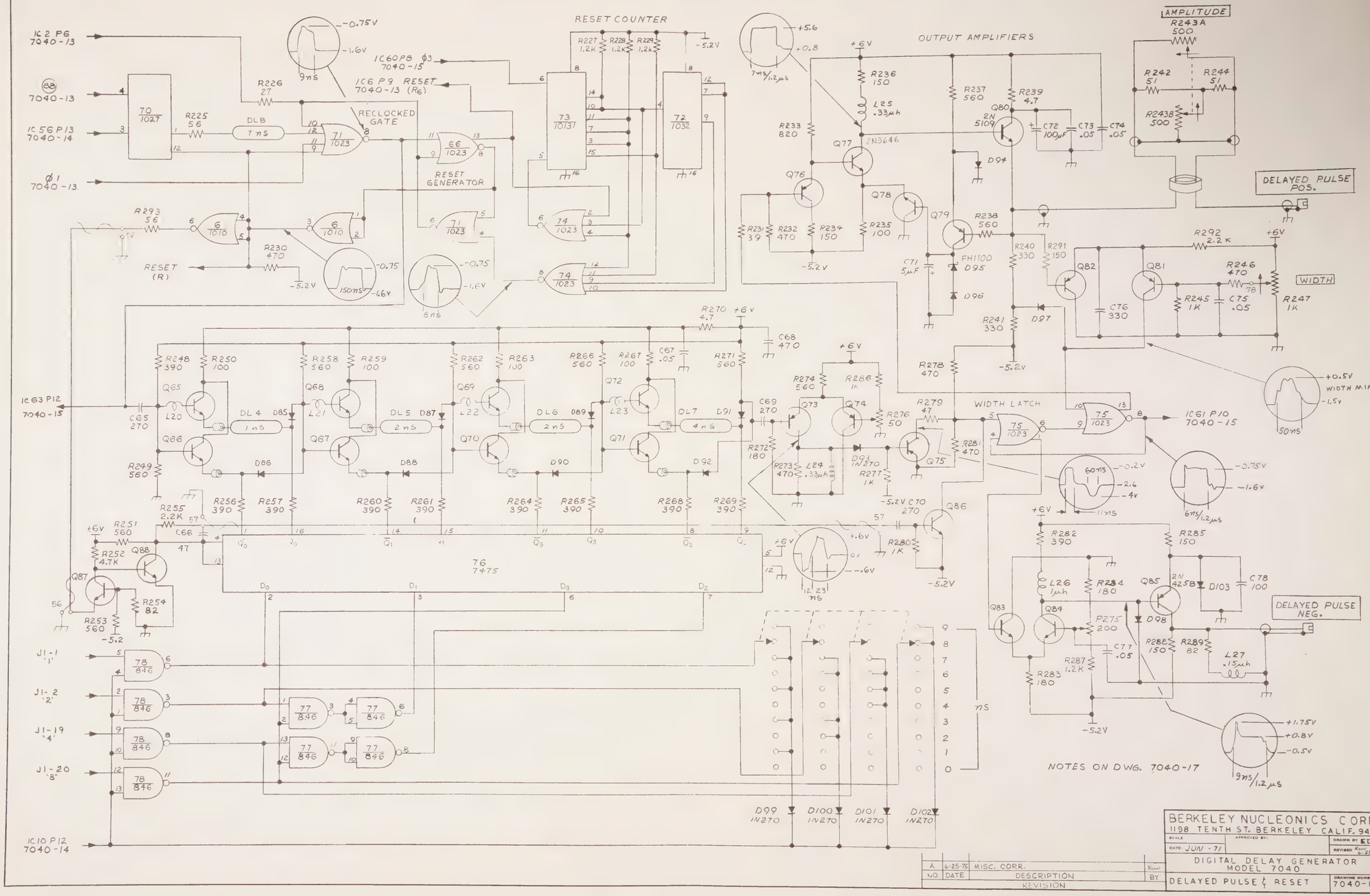
NO	DATE	DESCRIPTION REVISION	BY
A	6-25-75	MISC. CORR.	

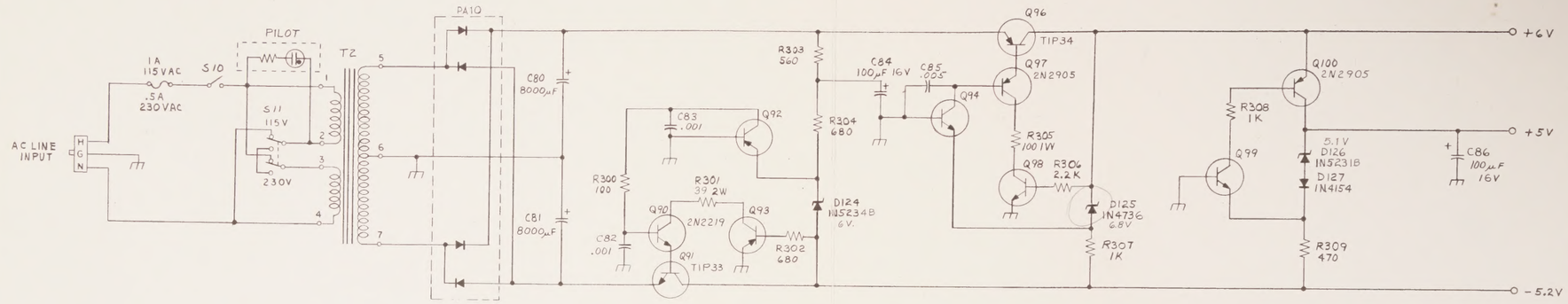
BERKELEY NUCLEONICS CORP.
1198 TENTH ST. BERKELEY CALIF. 94710

SCALE: | APPROVED BY: | DRAWN BY: E.D.R.
DATE: APRIL-71 | REVISED: 6-25-75

DIGITAL DELAY GENERATOR MODEL 7040

INITIAL, GATE, GATED CLOCK | DRAWING NUMBER: 7040-15A


RESET COUNTER
OUTPUT AMPLIFIERS
AMPLITUDE
R243A 500
DELAYED PULSE POS.
WIDTH
WIDTH LATCH
DELAYED PULSE NEG.
RECLOCKED GATE
RESET GENERATOR
RESET (R)
IC 2 P6 7040-13
IC 56 P13 7040-14
IC 60 P8 φ3 7040-15
IC 6 P9 RESET 7040-13 (R6)
IC 63 P12 7040-15
IC 61 P10 7040-15
IC 10 P12 7040-14
J1-1
J1-2
J1-19
J1-20
NOTES ON DWG. 7040-17
BERKELEY NUCLEONICS CORP.
1198 TENTH ST. BERKELEY CALIF. 94710
DIGITAL DELAY GENERATOR
MODEL 7040
DELAYED PULSE & RESET
DRAWING NUMBER 7040-16A
A 6-25-75 MISC. CORR.
NO. DATE DESCRIPTION REVISION BY



TYP. POWER SUPPLY PERFORMANCE
RIPPLE .120 Hz
LESS THAN 10 mV PP
REGULATION LESS
10 mV 102V TO
126 V LINE

NOTES

UNLESS OTHERWISE NOTED ALL

1) RESISTOR 1/4W 5% VALUE IN OHMS
   CAPACITORS VALUES
   a) LESS THAN ONE IN μFD
   b) GREATER THAN ONE IN pFD
   TRANSISTORS
   NPN ARE 2N3646
   PNP ARE 2N3640
   DIODES ARE IN4152
2) ALL UNUSED GATE INPUTS ARE RETURNED TO -5.2V

   15 / 1023 — IC IDENTIFICATION NUMBER / IC MANUFACTURERS TYPE NUMBER
3) NUMBERS WITHIN CIRCLES (82) INDICATE WIRE POINT
4) COAXIAL LINES ARE 50Ω IMPEDANCE
5) INTERCONNECTION BETWEEN DRAWINGS AS IC61P3 / 7040-16
   INDICATES CONNECTION TO IC61 PIN3 ON DWG. 7040-16

NO.	DATE	REVISIONS DESCRIPTION	BY
A	6-25-75	MISC. CORR.	RWO

BERKELEY NUCLEONICS CORP.
1198 TENTH ST. BERKLEY CALIF. 94710

SCALE:	APPROVED BY:	DRAWN BY EDR
DATE MAY-71		REVISED

DIGITAL DELAY GENERATOR
MODEL 7040

POWER SUPP. & NOTES — DRAWING NUMBER 7040-17A